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PREFACE

This report is an initial review of Department of Energy (DOE) microelectronics capabilities related to Department of Defense (DOD) needs, and documents the results of a preliminary survey of opportunities where DOE and DOD can leverage mutual microelectronics capabilities. The study was conducted under the Independent Research Program of the Institute for Defense Analyses (IDA) as Central Research Project 9001-520, Application of DOE Microelectronics Capabilities to DOD Needs. It serves as a basis to more fully articulate DOD opportunities for using DOE microelectronics technology and to identify strategies for realizing these opportunities.

We would like to acknowledge the support and contributions of Norman Kriesman of DOE; Linda Wilson of SEMATECH; Alastair McDowell of Lucent Technologies; Kenneth H. Bauer of Kansas City Area Office, DOE; David Atwood of Lawrence Berkeley National Laboratory; Tony Bernhardt of Lawrence Livermore National Laboratory; Mel Duran of Los Alamos National Laboratory; Gary Alley of Oak Ridge National Laboratory; and Dave Myers and Richard Stulen of Sandia National Laboratories; and Paul O'Connor and D. Peter Siddon of Brookhaven National Laboratory.

We also wish to thank the Mid-Atlantic Technology Application Center for the right to extract and present data concerning DOE laboratories and facilities contained in its Federal Laboratories Database.

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EXECUTIVE SUMMARY

Background

DOD has long recognized the critical importance of microelectronic devices and the underlying microelectronics manufacturing infrastructure (including manufacturing equipment and materials) necessary to achieve qualitative superiority and maintaining general military preparedness. Because microelectronics technology serves as a "force multiplier," United States defense planners increasingly rely upon it to provide significant advantage over all potential adversaries. But in the context of large and rapidly growing commercial microelectronics markets, defense specialty suppliers continue to scale back operations or abandon the defense business. A survey of microelectronics capabilities resident in the DOE laboratory system was undertaken to determine the potential for DOE capabilities to assist in fulfilling the DOD microelectronics requirements.

DOE has 39 laboratories and related facilities, including 9 large "multiprogram" laboratories and 8 major "single-program" laboratories. The combined DOE laboratories represent a significant national resource with technical capabilities and assets that are world-class and in some cases unique. The weapons laboratories, Sandia National Laboratories, Lawrence Livermore National Laboratory, and Los Alamos National Laboratory, have historically conducted microelectronics research and development (R&D) in support of their primary mission requirement, the production of nuclear weapons. However, by the late 1980s, the U.S. semiconductor industry recognized that DOE laboratories could make a significant contribution to microelectronics competitiveness. As a result, a number of industry-laboratory efforts were initiated.

Scope

This initial analysis of a selected set of DOE laboratories and facilities was conducted to focus on three technical areas that DOD uses in the annual Defense Technology Area Plan (DTAP) for electronics: microelectronics, electronic materials, and electronic integration technology. The purpose of the preliminary assessment was to determine the extent and availability of DOE laboratory capabilities and resources available to meet DOD mission

requirements, with an emphasis on science and technology (S&T) and prototyping capability. Also included in the electronics DTAP, but not addressed in this assessment are the sub-areas of radio frequency (RF) components and electro-optics. These technology sub-areas have significant microelectronics aspects and should therefore be considered in any further evaluation of DOE laboratory capabilities.

Methodology

The Institute for Defense Analyses (IDA) study team identified the opportunities where DOD can leverage DOE microelectronic technology capabilities and mutual development opportunities where DOE capabilities and facilities may address identified DOD S&T requirements. The current DOE laboratory capabilities and facilities in microelectronics were identified through open literature and several technology databases. Seven key DOE[1] laboratories with microelectronics capabilities were selected and visited by the team. Follow-up interviews with representatives of DOE, DOD, and the commercial microelectronics industry provided clarification where required.

Findings

A summary of DOE microelectronics capabilities found at the selected facilities is presented in Table ES-1. Capabilities were found at other laboratories, such as Ames and Argonne National Laboratories laboratories, but this assessment only presents primary findings for the selected facilities. The preliminary information gathered by the IDA research team indicates that DOE laboratories and facilities have strong microelectronics capabilities in a wide range of areas relevant to the DTAP areas examined.

[1] The selected DOE laboratories were Brookhaven, Kansas City Plant, Los Alamos, Lawrence Berkeley, Lawrence Livermore, Oak Ridge, and Sandia.

Table ES-1. DTAP Technologies of Major DOE Facilities

Area and Sub-Areas	Brookhaven National Lab	Kansas City Plant	Los Alamos National Lab	Lawrence Berkeley National Lab	Lawrence Livermore National Lab	Oak Ridge National Lab	Sandia National Labs
Microelectronics							
Mainstream silicon technology	X			X	X	X	X
Expanded Performance Processes, Devices and Circuits		X	X			X[a]	X
Microelectromechanical Systems	X			X	X		X
Electronic Materials							
Chemical synthesis			X				X
Bulk and thin film/ nanostructure materials fabrication	X		X		X	X	X
Development of materials fabrication processes	X		X	X	X		X
Electrical, optical, structural, morphological, and chemical characterization	X		X	X	X	X	X
Electronics Integration Technology							
Design, Test and Quality Assurance		X	X		X	X	X
Packaging, Interconnect and Assembly		X	X		X	X	X
Power			X				

a. Provides fabless design, i.e., uses best outsource capability available.

While collecting data on capabilities and visiting facilities, information on how DOE and DOD actually manage, coordinate and perform microelectronics technology work started to emerge. The following observations highlight what was found during this study.

Observations

1. DOE does not have a centralized headquarters planning functions for microelectronics.
2. DOE recently initiated an S&T strategic planning process. Primarily, it is a high-level reporting activity, but it lacks specific microelectronics technology focus. The initial DOE database contains approximately 11,000 projects in all technology areas.
3. There is limited, informal coordination between DOE and DOD concerning microelectronics R&D and life cycle planning, and funding processes.
4. DOD lacks an integrated view of DOE laboratory capabilities and resources relevant to DOD microelectronics requirements. DOD has not generally considered the DOE laboratories as a source of microelectronics technology, at times delaying access to key miniaturization and reliability improvement technologies.
5. DOD microelectronics planning has formal mechanisms for conducting planning and reporting among the three Services, the Defense Special Weapons Agency, the Defense Advanced Research Projects Agency, and the Ballistic Missile Defense Office. DOE has no such mechanisms.
6. DOD does not participate in the SEMATECH microelectronics project database, contributing to an incomplete view of government and industry microelectronics investments. By not participating in this project, DOD is unable to benefit from the planning information provided by DOE and commercial industry in this database.

Conclusion and Recommendations

As a result of our preliminary analysis, we concluded that a number of opportunities exist for cooperative DOD-DOE activities in microelectronics. To take advantage of these opportunities, DOD should consider the following:

1. Explore DOE laboratory capabilities for relevant S&T efforts as well as prototype production of unique defense electronics.
2. Identify mechanisms to increase involvement in joint DOD and DOE microelectronics planning and investment.
3. Be specifically involved in major DOE efforts in electronic materials, lithography and related micro-manufacturing processes, radiation hardness, and electronic integration technologies (e.g., multi-chip modules).

1. INTRODUCTION

1.1 PURPOSE

The purpose of this preliminary study is to work towards identifying near- and long-term strategic areas for United States Department of Defense (DOD) and Department of Energy (DOE) to mutually leverage microelectronic technology development capabilities and investments. The scope of microelectronic technology considered spans three key Defense Technology Area Plan (DTAP) electronics areas: microelectronics, electronic materials, and electronic integration technology. This document contains the preliminary results identifying the scope of DOE capabilities and facilities and the potential relationships to DOD microelectronics requirements.

Research staff members of the Institute for Defense Analyses (IDA) conducted a preliminary survey of the DOE laboratories and facilities to determine microelectronics capabilities and resources available to support DOD needs. DOD mission requirements, as stated in various DOD planning documents,[1] provided a view of DOD microelectronics requirements. The study team followed the initial research with a visit to the following DOE laboratories and facilities with significant microelectronic capability:

- Allied Signal Kansas City Plant, Kansas City, Missouri
- Brookhaven National Laboratory, Upton, Long Island, New York
- Lawrence Berkeley National Laboratory, Berkeley, California
- Lawrence Livermore National Laboratory, Livermore, California
- Los Alamos National Laboratory, Los Alamos, New Mexico
- Oak Ridge National Laboratory, Oak Ridge, Tennessee
- Sandia National Laboratories, Kirtland Air Force Base, Albuquerque, New Mexico; Livermore and San Jose, California, sites

[1] The DOD microelectronics needs are summarized in Appendix B and in references [DTAP 97], [TAR 97].

The IDA study team identified the opportunities where DOE and DOD can leverage mutual microelectronic technology capabilities and development interests by comparing DOE capabilities and facilities with identified DOD Science and Technology (S&T) requirements. The current DOE laboratory capabilities and facilities in microelectronics were identified through open literature, including Internet sources; materials published by the laboratories; access to specialized databases; and interviews with representatives of DOE, DOD, commercial microelectronics industry, and universities.

Databases of federal laboratories capabilities, facilities, and projects were obtained from Mid-Atlantic Technology Application Center. A national database of electronic projects prepared by SEMATECH (beta release) was used to identify a partial listing of projects and potential capabilities. Essential data were collected during technical interchange meetings at Brookhaven National Laboratory, the Allied Signal Kansas City Plant, Lawrence Berkeley National Laboratory, Lawrence Livermore National Laboratory, Los Alamos National Laboratory, Oak Ridge National Laboratory, and Sandia Laboratories.

The study team identified specialized DOD microelectronics technology needs based on an analysis of the Defense Technology Area Plan [DTAP 97] in microelectronic areas. The relationship of DOE capabilities and facilities to DTAP technology areas was established.

1.2 STUDY TASKS

A summary of the methodology used during the study follows:

a. Data collection

   1. Interview DOE personnel at DOE headquarters.
   2. Send letters and request information from all major DOE laboratories.
   3. Review DOE, SEMATECH, and MTAC databases.
   4. Review open literature sources including the world wide web.

b. Analyses

   1. Analyze DOE microelectronics capabilities.
   2. Analyze DOD microelectronics needs (primarily through the DTAP).
   3. Compare the DOE capabilities to the DOD needs.

1.3 DTAP MICROELECTRONICS AREAS

The DTAP identifies Microelectronics, Electronic Materials, Electronic Integration Technology, RF Components, and Electro-optics as essential to meeting defense mission requirements [DTAP 97]. This study focused on Microelectronics, Electronic Materials, and Electronic Integration Technology. A detailed discussion of these DTAP areas is found in Appendix B.

RF Components and Electro-optics areas have significant microelectronics aspects and therefore should be considered in any further evaluation of DOE capability. Table 1 provides a summary of all DTAP electronic sub-areas.

Table 1. DTAP Electronics Taxonomy

Major Area	Sub-Area
Areas and Sub-Areas Covered by IDA Study	
Microelectronics	Mainstream silicon technology Expanded performance processes, devices, and circuits Microelectromechanical systems
Electronic Materials	Chemical synthesis Bulk and thin film/nanostructure materials fabrication Development of materials fabrication processes Electrical, optical, structural, morphological, and chemical characterization
Electronics Integration Technology	Design, test, and quality assurance Packaging, interconnect, and assembly Power
Areas **Not** Covered by IDA Study	
RF components	Integrated computer-assisted design (CAD) (solid state and vacuum electronics) High-density packaging Wideband, high power Highly efficient vacuum tube and solid state amplifiers Mixed signal integrated circuits (ICs) Materials for frequency control MMW integrated circuits Compact multifunction antennas

Table 1. DTAP Electronics Taxonomy (Continued)

Major Area	Sub-Area
Electro-optics	Photonics Displays Lasers Focal plane arrays (FPAs) Electro-optical (EO) device technology

1.4 DOCUMENT ORGANIZATION

Chapter 2 provides background and context for DOD microelectronics requirements.

Chapter 3 presents an overview of the history and missions of the individual DOE laboratories and facilities visited or contacted, and a list of the core competencies for each site.

Chapter 4 discusses current military microelectronics technology life cycle, in terms of how military microelectronics technology is developed, how it is inserted into procured systems, and current investment strategies by DOD.

Chapter 5 provides the findings, observations, conclusion, and recommendations.

Appendix A contains descriptions of DOE facilities and labs taken from the Mid-Atlantic Technology Application Center Federal Laboratories Database, and used with permission. The descriptions of the microelectronics capabilities for each facility are given for each of the relevant DTAP categories.

Appendix B presents DOD needs focused on Defense Technology Objectives (DTOs). The DTOs relevant to microelectronics are summarized, and the current DOD investment strategy, which reflects how DOD is currently trying to meet these needs, is discussed.

Appendix C describes DOE laboratory efforts concerning Extended Ultra-Violet Lithography (EUV), for mass producing integrated circuits with less than 0.15 μm feature size.

2. BACKGROUND

DOD has long recognized the critical importance of microelectronic devices and the underlying microelectronics manufacturing infrastructure (including manufacturing equipment and materials) to achieving qualitative superiority and maintaining general military preparedness. Because microelectronics technology serves as a "force multiplier," U.S. defense policy is increasingly relying on it to provide significant advantage over potential adversaries.

The DOD examines its needs on an ongoing basis, and develops strategies for addressing those needs. The Joint Chiefs of Staff's Joint Vision 2010 [Joint Vision 96] defines a common direction and set of operational concepts. In particular, it examines how technological advances and information superiority can lead to new and significantly improved capabilities. The Joint Vision 2010 identifies four key concepts:

- **Dominant Maneuver:** The multidimensional application of information and maneuver capabilities to provide coherent operations of air, land, sea, and space forces throughout the breadth, depth, and height of the battlespace to seize the initiative and control the tempo of the operation to a decisive conclusion.
- **Precision Engagement:** The capability to accurately locate the enemy, command and control friendly forces, precisely attack key enemy forces or capabilities, and accurately assess the level of success.
- **Full Dimensional Protection:** The ability to protect our forces at all levels and obtain freedom of action while they deploy, maneuver, and engage an adversary.
- **Focused Logistics**: The capability to respond rapidly to crises, shift warfighting assets between geographic regions, monitor critical resources enroute, and directly deliver tailored logistics at the required level of operations.

In order to achieve these capabilities, the Joint Staff have developed twelve high-priority areas, called Joint Warfighting Capability Objectives (JWCOs) [Joint Vision 96].

The following twelve JWCOs are used by DoD to develop strategies and prioritize its activities [DSTS 96, JWSTP 97]:

- **Information Superiority.** Combines the capabilities of intelligence, surveillance, and reconnaissance (ISR) along with command, control, communications, computers, and intelligence (C^4I) to acquire and assimilate information needed to dominate and neutralize adversary forces and effectively employ friendly forces. Includes the capability for near-real-time awareness of the location and activity of friendly, adversary, and neutral forces throughout the battlefield area. Also includes a seamless, robust C^4 network linking all friendly forces to provide common awareness of the current situation throughout the battlefield area.
- **Precision Force.** Capability to destroy selected targets with precision while limiting collateral damage. Includes precision guided munitions, surveillance, targeting, and "sensor-to-shooter" C^4I capabilities necessary for responsive, timely force application.
- **Combat Identification.** Capability to differentiate potential targets as friend, foe, or neutral in sufficient time, with high confidence, and at the requisite range to support weapons release and engagement decisions.
- **Joint Theater Missile Defense.** Capability to use the assets of multiple Services and Agencies to detect, track, acquire, and destroy enemy theater ballistic missiles and cruise missiles. Includes the seamless flow of information on missile launches by specialized surveillance capabilities, through tracking by sensors from multiple Services and agencies, to missile negation or destruction.
- **Military Operations in Urban Terrain.** Capability to operate and conduct military operations in built-up areas and to achieve military objectives with minimum casualties and collateral damage. Includes precise weapons, surveillance, navigation, and communications effective in urban areas.
- **Joint Readiness.** Capability to enhance readiness for joint and combined operations, including capabilities for enhanced simulation for training.
- **Joint Countermine.** Capability for assured, rapid surveillance, reconnaissance, detection, and neutralization of mines to enable forced entry by expeditionary forces. Included is the capability to control the sea and to conduct amphibious and ground force operational maneuvers against hostile defensive forces

employing sea, littoral, and land mines. For land forces, dominance means the ability to conduct in-stride tempo operations in the face of severe land mine threats.

- **Electronic Warfare.** Capability to disrupt or degrade an enemy's defenses throughout the area and time required to permit the deployment and employment of U.S. and allied combat systems. Includes capabilities to deceive, disrupt, and destroy the surveillance and command and control systems as well as the weapons of an enemy's integrated air defense network. Also includes capabilities for recognizing attempts by hostile systems to track or engage.
- **Information Warfare.** Capability to achieve information superiority by affecting an adversaries information, information systems, information-based processes, and computer-based networks while defending one's own information, information-based processes, information-based systems, and computer-based networks.
- **Chemical/Biological Agent Detection.** Capability for standoff detection of biological agents is our single most pressing need. Capabilities in both point and standoff detection of chemical and biological agents, combined with the ability to assess and disseminate threat information in a timely manner, are critical to protecting fielded forces.
- **Real-time Logistics Control.** Capability for near real-time visibility of people, units, equipment, and supplies which are in storage, in process, in transit, or in theater, and the ability to act on this information.
- **Counterproliferation.** Capability to 1) detect and evaluate the existence of a manufacturing capability for weapons of mass destruction (WMD), and 2) identify and assess the weapon capability of alert and launched WMDs on the battlefield to permit the proper level of counterforce to be exerted promptly. Includes counterforce against hardened WMD storage and production facilities.

In addition to these objectives, DOD has defined four key considerations as being of high priority in decision making and need to be considered broadly:

- **Affordability**. Where appropriate, Science and Technology (S&T) projects must focus on increasing the effectiveness of a capability and decreasing cost, increasing operational life, and incrementally improving material through planned upgrades.

- **Dual Use.** The S&T program must contribute to building a common industrial base by using commercial practices, processes, and products, and by developing, where possible, technology that can be the base for both military and commercial products and applications.
- **Accelerated Transition.** Advanced Concept Technology Demonstrations (ACTDs) are a key element in the S&T program to focus science and technology on supporting military needs and problems, expediting transitions, and providing a sound basis for acquisition decisions.
- **Strong Technology Base.** Basic and applied research generate DoD's legacy to tomorrow's warfighter. Accordingly, it is imperative to maintain a stable technology base investment to develop options for the truly long term beyond the threats, situations, and budgets that we can predict.

It is of vital interest to note that microelectronics plays a central role in meeting virtually all of the JWCOs. It also is of further note that this same technology is at the heart of the four high-priority considerations. These articulations all point to the need for DOD to have good access to the full range of domestic and selected[1] foreign sources for microelectronics capabilities.

The way that DOD accesses microelectronics technology has changed dramatically over the last two decades. Prior to this period, DOD played a pivotal role in the advancement of microelectronics and dominated the development of the industry, being its biggest customer. However, over the last 20 years, the DOD has seen its dominant customer position decrease from 20 percent in 1975 to less than 3 percent today [ICE 96]—the result of the exploding demand for commercial microelectronics combined with flat defense procurement. During this same time, the cost of microelectronic research, development, and manufacturing has risen significantly. The capital cost for the next-generation plant for high-volume production of microcircuits is expected to be about $2 billion [ICE 96]. A minimum domestic plant will have at least a capital cost of $100 million[2]. Defense microelectronics suppliers are now abandoning the defense market, lured by growing and profitable commercial markets. Suppliers are unable to foresee any change in the high investment cost and low volume of defense business.

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[1] Consistent with current U.S. DOD policy.

[2] IDA internal studies indicate that it currently costs over $100M to capitalize a plant, including equipment, clean room and hookup of required services. This result is independently supported by the SEMATECH cost models and actual plant construction surveys.

Consequently, DOD must increase its reliance on commercial industry for its microelectronic components. Commercial industry, however, is not immediately prepared to meet all DOD needs, and DOD is not yet accustomed to dealing with all of commercial industry practices. Appropriate use of commercial capabilities offers DoD important advantages, enabling DoD to capitalize on the economies of scale in the commercial market to achieve significantly lower costs and often obtain more advanced technology. While DOD has recently implemented policies allowing defense acquisitions to make greater use of commercial products, it is the higher-volume commodity approach of mainstream commercial suppliers that makes it increasingly difficult for commercial industry to meet defense-specific, low-volume needs. Although DOD may benefit from increased access to commercial microelectronics, it is faced with a consolidation of its defense microelectronic supplier base—which could have a severe effect on current and future defense systems [DOD 96].

Two key issues are: (1) How and where can DOD best make use of commercial microelectronics capabilities, and (2) Where do specialized defense needs still exist that cannot or will not be met by commercial suppliers?

As resources in support of defense microelectronics requirements continue to be scaled back, it becomes more important that DOD consider it's relationship with DOE and the role DOE plays in meeting DOD needs. In particular:

- Is DOD fully aware of the microelectronics capabilities resident in the DOE laboratories (e.g., technology, facilities, and equipment), and are there significant opportunities that are being missed to employ these capabilities to meet DOD mission requirements?
- Does DOD adequately take these DOE capabilities into account when undertaking its strategic planning exercises (e.g., the Defense Science and Technology Strategy, Defense Technology Plan, Detailed Technology Area Plan for Electronics, Electron Devices Technology Area Review for Microelectronics Subarea, and individual program planning) and funding initiatives?

3. DOE LABORATORIES

3.1 HISTORY OF DOE LABORATORIES

The history of DOE's laboratories dates back to World War II when it was necessary to establish leading-edge nuclear research and production facilities in support of the Manhattan Project. Several of DOE's largest laboratories were established during this time. Shortly thereafter, with the advent of the Cold War, other key laboratories and related facilities were organized to develop and produce nuclear weapons. The laboratories have been a supplier of leading research and research scientists in many disciplines. In particular, DOE laboratories have been involved in microelectronics or related materials and manufacturing science and technologies for decades.

Today, DOE manages the nation's largest system of federal laboratories with a combined FY95 research budget of approximately $6.6 billion and a work force of more than 57,000 [DOE Tech Xfr 95]. Laboratory core missions focus on energy resources, national security, science and technology, and environmental quality [DOE Tech Xfr 95]. These core missions support DOE's primary responsibility: management of nuclear and non-nuclear federal energy policy and programs [Fehner 94].

DOE has 39 laboratories and related facilities, including nine large "multiprogram" laboratories and eight major "single-program" laboratories.

The combined DOE laboratories represent a significant national resource with technical capabilities and assets that are world-class and in some cases unique. Because of the expense and effort spent in the establishment of this laboratory system, it is unlikely that many of its resident capabilities could ever be recreated.

The "weapons" laboratories (Sandia National Laboratories, Lawrence Livermore National Laboratory, and Los Alamos National Laboratory) have historically conducted microelectronics research and development in support of their primary mission requirement, the production of nuclear weapons. However, by the late 1980s, industry recognized that the DOE laboratories could make a significant contribution to microelectronics competitiveness and studied the question of whether DOE resources could be mobilized to

"leverage facilities, capabilities, and results on a national level" [DOE Semi 93]. As a result, in recent years, a number of industry-laboratory efforts been initiated. For example, "in 1993, Sandia's expenditures for microelectronics-related programs totaled $106 million, much of which supported collaborative work with commercial industry." [DOE Semi 93]

Most of these efforts have been organized as Cooperative Research and Development Agreements (CRADAs). A series of CRADAs, jointly funded by DOE and industry, has enabled Sandia to cooperate with SEMATECH since 1989 concerning equipment improvement and enhancement through basic equipment and process modeling, software improvement, equipment benchmarking, and support for ergonomics, tribology, and reliability projects.[1] The Semiconductor Research Corporation (SRC) and the National Laboratories had a $100 million, five-year CRADA aiming to preserve the U.S. lead in semiconductor manufacturing.[2] In addition to these activities, DOE had provided approximately $81 million by the end of FY93 to Sandia, Los Alamos, and Lawrence Livermore in support of a range of other microelectronics-related CRADAs [DOE Semi 93].

3.2 KEY DOE MICROELECTRONICS CAPABILITIES

This section provides a synopsis of DOE microelectronic capabilities and facilities that match DTAP requirements in the microelectronics, electronics materials, and electronics integration technology categories discussed previously in Table 1, "DTAP Electronics Taxonomy," on page 3. The research and development capabilities described range from science through production. The facilities likewise range from research laboratories to production plants. Specific DTAP areas and sub-areas are listed for each facility. Information was gathered from Internet[3] and commercial and government database resources. Seven DOE laboratories with the most prominent microelectronics activities were selected and visited. This assessment focuses on those laboratories, although relevant work was also identified at Ames and Argonne National Laboratories. For completeness, the capabilities of these two laboratories are documented in Table 2 and described in detail in Appendix A.

Key DOE microelectronics research, development, or manufacturing capabilities are listed in Table 2. Detailed descriptions of laboratory capabilities can be found in Appen-

[1] IDA unpublished study report on semiconductor manufacturing materials and equipment.

[2] Ibid.

[3] The best World Wide Web site to access information on DOE facilities is the DOE Technology Information Network, http://www.dtin.doe.gov.

dix A. Of special note is a brief analysis of laboratory activity concerning the development of Extended Ultra-Violet (EUV) lithography technology (discussed in more detail in Appendix C). Significant and coordinated efforts in the EUV area have been undertaken by several laboratories.

Table 2. Key DOE Microelectronic Capabilities

DOE Facility	Capabilities
Ames	Advanced materials synthesis and processing. Preparing ultra high-purity and well-characterized metals, alloys, composites, and single crystals.
Argonne National Laboratory	Advanced materials characterization through EXAFS efforts at Brookhaven National laboratory and the new advanced light source at Argonne.
Brookhaven National Laboratory	National Synchrotron Light Source is the world's largest facility dedicated to producing synchrotron light that is applied to 13-nanometer EUV lithography. Small-scale research in hybrid and monolithic microcircuit design and test; data acquisition system design; silicon detector design, fabrication, and test; and silicon micromachining.
Allied Signal Kansas City Plant	Design, fabricate, and test hybrid microcircuits and multichip modules and to package semiconductor devices in a production environment. This capability includes state-of-the-art circuit design and analysis equipment. These RF, digital, and analog microelectronic devices have been utilized in products such as radars, firesets, programmers, and secure systems where miniaturization and high-reliability electronic packaging are required. 13,000 sq. ft. of Class 100 and Class 10,000 cleanrooms and can produce medium-scale production quantities of up to hundreds per month of individual part numbers. Production and support organizations are capable of handling classified material. Integrated support services concerning test equipment design and fabrication, metrology, materials analysis, and electronic component failure analysis are available. Fabrication of RF and logic hybrid microcircuits and MCMs utilizing a wide variety of substrates, semiconductor die (including diodes, transistors, LSI circuits and ASICs in silicon and gallium arsenide), appliqué components, and intraconnection methods.

Table 2. Key DOE Microelectronic Capabilities (Continued)

DOE Facility	Capabilities
Lawrence Berkeley National Laboratory	Design and development of charged particle instruments including accelerator, ion beam lithography, plasma, and thin film tools. Complete semiconductor characterization facilities, and semiconductor processing and detector fabrication capabilities, producing infrared and x-ray sensors using germanium, silicon, gallium arsenide, indium phosphide, and zinc selenide. Fabrication of high aspect ratio microstructures using LIGA. Capabilities in the areas of crystal cutting, lapping and polishing, chemical etching, ion implantation, tin-film deposition, and microfabrication techniques. EUV optics, design, metrology, and fabrication expertise. User facility with a third-generation synchrotron optimized as the highest brightness source of soft x-ray and vacuum ultraviolet photons.
Lawrence Livermore National Laboratory	Silicon front-end-of-line processing including shallow junction formation, bulk process modeling, and deposition and etching; interconnect, including metal and dielectric materials and processes, and interconnect reliability issues; equipment design and modeling; lithography; including light sources, optics and precision motion control; and packaging, including electronic, optoelectronic, and package interconnect modeling and simulation. EUV radiation production, optical design, EUV mirror technology, reflective mask technology and advanced metrology of high precision optics. Electronic packaging, modeling, and simulation. Lawrence Livermore has over 12,000 sq. ft. of Class 10 to 100 clean rooms housing fabrication equipment for silicon processing and micromachining, III-V semiconductor applications, optoelectronics and guided wave photonics, and IC packaging. This lab has extensive facilities (30,000 sq. ft.) for materials characterization.

Table 2. Key DOE Microelectronic Capabilities (Continued)

DOE Facility	Capabilities
Los Alamos National Laboratory	Theory and modeling of advanced materials and processes utilizing high-performance computing capabilities; development and support of 3-D grid servers (LaGriT) with unstructured grids and automatic mesh refinement for use by TCAD tools for predictive modeling and simulation of 0.1-0.25 μm devices; 3-D front-tracking grain growth simulations for interconnect reliability predictions; ion implantation modeling using molecular dynamics simulations; 3-D topological modeling tools for CVD processes; and interconnect signal integrity modeling. Advanced high-dielectric-constant materials for gate-stack, charge-storage and sensing applications; organic polymeric materials for electronic technologies; self-assembly (organic and inorganic) of monolayers and heterostructures for electronic, sensing, lithographic, and bio technologies; thin film and interface technology (organic and inorganic materials); and advanced multi-resolution signal processing analysis. Rapid prototype development of microelectronic components for ASIC and MCM; and custom CAD design development software which reduces non-recurring engineering costs associated with ASIC and MCM development.
Oak Ridge National Laboratory	In-house design of digital, RF and microwave microelectronics, applying state-of-the-art synthesis and simulation tools (actual fabrication is outsourced). Radiation hardening of electronics through circuit/device design and packaging. Design and packaging techniques to mitigate against harsh environments. Multidisciplinary research focuses on several important classes of materials, including ceramics and composites, metals and alloys, superconductors, and thin films. "Z-contrast" electron microscopes enable viewing a material's complex atomic structure with a resolution of 1.3 angstroms. Development of complex custom ASIC for digital and RF applications. Materials synthesis, processing, and characterization through modeling and performance evaluation.

Table 2. Key DOE Microelectronic Capabilities (Continued)

DOE Facility	Capabilities
Sandia National Laboratory	Capabilities include technology required for development fabrication, and production of microelectronic and photonic devices. Distinguishing strengths of this competency include materials growth and development, device design, fabrication technologies for silicon and compound semiconductor devices, advanced packaging technologies, and design of processes and equipment for the manufacture of integrated circuits, advanced manufacturing with extreme ultraviolet lithography, theory, modeling and simulation of chemically reacting flow. Major facilities that support electronics technology include the Center for Compound Semiconductor Technology, Advanced Manufacturing Processes Laboratory, Advanced Materials Research Laboratory, the Microelectronics and Photonics Center, and the Center for MicroelectronicsTechnologies/Microelectronics Development Laboratory. The Microelectronics Development Laboratory (MDL), with a major donation from the IBM Corporation of equipment and technology, provides 74,000 sq. ft. which includes 30,000 sq. ft. of cleanroom space with 12,500 sq. ft. of class-1 clean space in 22 separate clean rooms. The IBM equipment and technology donation provides a state-of-the-art submicrometer silicon IC research and development line supporting the total semiconductor development cycle.

4. CURRENT DOD MICROELECTRONICS INVESTMENT STRATEGY

4.1 CURRENT SERVICE/OSD INTERNAL INVESTMENT STRATEGIES

Currently, each of the Services and OSD control their own investments and make basic direction and planning decisions. Each Service is characterized by the following:

- Laboratory staffs, with in-house work being performed in microelectronics.
- Strategic and planning groups that coordinate the internal plans and budgets for projects.
- Development and publication of a Service-specific strategy that details the Service strategy for S&T work in all areas.
- Separate budget authority under which microelectronics work is performed.

Generally, each Service invests in a broad range of areas for modest sums. The individual investment areas are managed independently and are not integrated. In some cases, there will be an explicit and/or strong connection between investments, such as in High T_c devices and SiC materials. Nevertheless, for the most part, investments are loosely coupled, fine grain, and small. Individual Service programs typically range in cost from $100,000 to $1 million annually.

DARPA, on the other hand, has a strategy of making integrated investments that have a tightly coupled program from basic research through technology development into technology demonstrations. Within a program there is tight coupling, but there is very loose coupling between programs. Typical DARPA programs range from $1-$10M annually in size (although some such as SEMATECH are $100 million per year).

Defense Special Weapons Agency (DSWA) primarily invests in a well-integrated program for radiation-hardened microelectronics. As this is a very specific DOD interest, the strategy and plan for this area is quite focused. DSWA spends less then $15 million per year in microelectronics.

The Ballistic Missile Defense Organization (BMDO) has had a variable influence on microelectronics. In general, BMDO has not had a separate technology focus on microelectronics, but has it as part of its vertically integrated programs that require extensive microelectronics. Significant microelectronics investments have been made by BMDO over the years, but most have been driven by their system-level programs and have been weakly coordinated with other BMDO and defense programs.

4.2 CURRENT SERVICE/OSD JOINT INVESTMENT STRATEGIES

There are a number of forums whereby joint Service and OSD strategies are developed:

- Deputy Director for Research and Engineering Technology Area Planning and Technology Area Review (DDR&E TAP/TAR) process
- Project Reliance
- Advisory Group on Electron Devices (AGED)
- Joint Programs

Each forum is discussed in further detail in the following sections.

4.2.1 DDR&E TAP/TAR Process

TAP/TAR is the latest to develop a DOD investment strategy for S&T. Currently, this plan is a single high-level document that covers all technologies, with about 15 pages devoted to microelectronics. The level of detail provided is insufficient to express an investment strategy, and instead provides a general investment philosophy. The overall process of planning is shown in Figure 1.

As shown in Figure 1, the individual Services plans are used as primary inputs to the Joint plans (Basic Research Plan (6.1) [BRP 97], Defense Technology Area Plan (6.2) [DTAP 97], and Joint Warfighting S&T Plan (6.3) [JWSTP 97]). These plans are then combined into a single Defense S&T plan [DSTS 96] which supports the Program Objective Memorandums (POM) and budget request process.

The plans are developed annually (in the winter) and are completed in sufficient time to influence the budget submissions from the Services. In the spring, a review of the previous years S&T results is presented and reviewed. Budget submission adjustments can be made at the last minute to reflect changes resulting from the review. Figure 2 shows the overall timeline of the process.

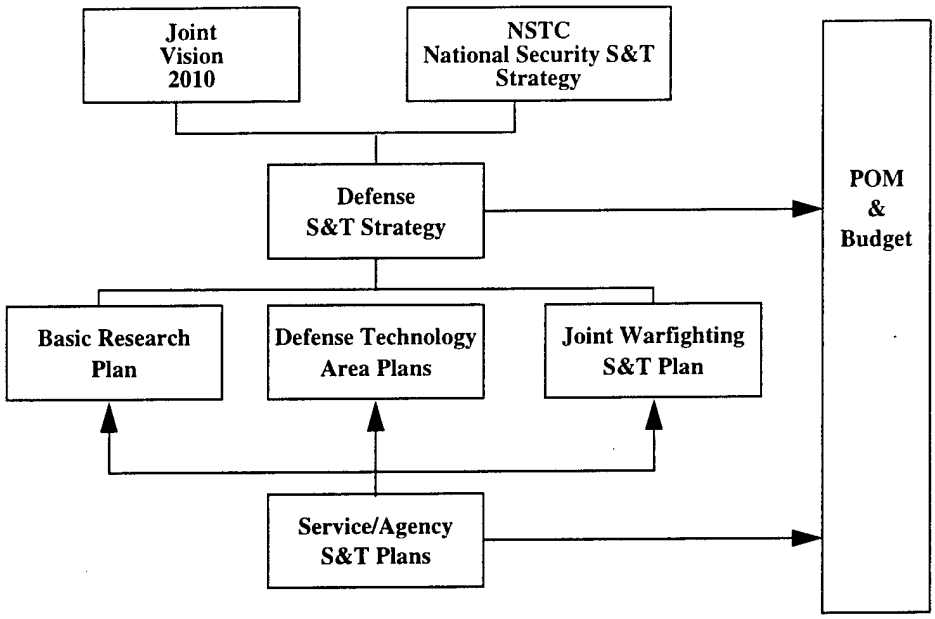

Figure 1. Science and Technology (S&T) Strategic Planning

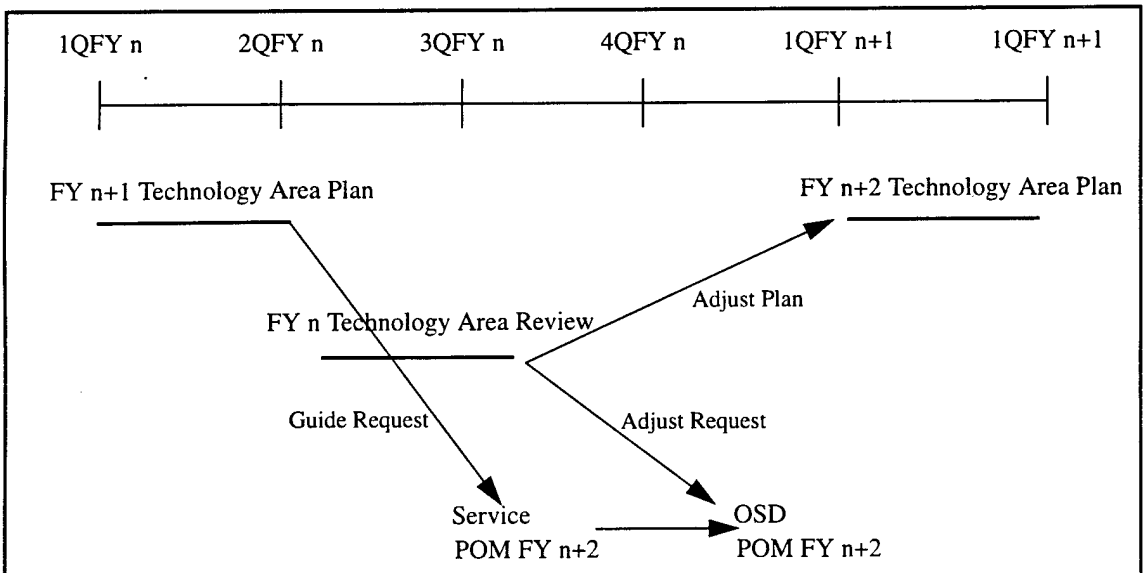

Figure 2. TAP/TAR Timeline

4.2.2 Advisory Group on Electron Devices (AGED)[1]

The Advisory Group on Electron Devices (AGED) is an organization that serves the Under Secretary of Defense for Acquisition and Technology, the DDR&E, the Director of the Defense Advanced Research Projects Agency, and the Military Departments by assisting in the strategic planning and management of effective and economical research and development in the field of electron devices. The objective of AGED is to provide guidance that will help ensure that critical DOD electron device needs are met in the most cost efficient and timely way.

Under the terms of its Charter, AGED is specifically required to perform a number of functions. The most important are as follows:

1. Providing on-going technical advice to the DDR&E, regarding electronic device programs, with an eye towards programs that can be immediately developed to meet future defense equipment and systems needs.
2. Advising the DDR&E on emerging technologies, significant advances, and new discoveries in the electron device field.
3. Acting as a "clearing house" for the interchange of electron device information within DOD, federal government agencies and government contractors, and industry.
4. Publishing Special Technology Area Reviews (STARs), focusing on a particular subarea or technology relevant to the electron device field.

AGED has three "Working Groups" composed of subject matter experts in a particular area of electron device technology. Working Group A concentrates on microwave components. Working Group B directs its attention to microelectronics. Working Group C centers its activities on electro-optics. A Main Group oversees and coordinates the activities of the Working Groups, and reviews their recommendations. The members are from industry, universities, and government with government members appointed by their respective organizations. Working Groups meet about every two months.

The AGED program is administered by the Secretariat for AGED, located at the Palisades Institute for Research Services, Inc., in Arlington, VA. The Palisades Institute facilitates the AGED program by providing a technically adept Secretary for each Working Group, by providing meeting space, and by publishing and distributing AGED materials. Each Secretary assists the Chairperson and Members of their respective Working Group by

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[1] This material is based on information from the AGED site on the World Wide Web, the DoD Advisory Group on Electron Devices (http://www.acq.osd.mil/ddre/aged/aged.html.)

coordinating activities, recommending subjects for review, and preparing documentation and materials of Working Group activities and recommendations.

In order to provide specialized information regarding research and development in the electron device field, AGED publishes materials and reports to support the DDR&E. The most significant of these reports are the STARs. STARs are often conducted as a joint effort between the three Working Groups and focus on a particular sub-area or technology relevant to the electron device field. STARs are conducted as a series of presentations made by speakers invited from universities, industry, and government who conduct research at the forefront of electron device technology. Recommendations from STARs are documented in report form. AGED also publishes an Annual Report that summarizes progress made during the preceding year on DOD electronics research and development activities and describes future electronics trends, programs, and goals.

4.2.3 Joint Programs

Joint programs are another way that joint strategies are developed. These areas are generally informal cooperative teams formed based on mutual interest and benefit. A recent example was the formation of a radiation hard microelectronics working group. This group identified a number of issues and made strategy recommendations to DDR&E; this eventually led to the formal creation of a joint Service/OSD Integrated Product Team to examine not only the S&T issues but the issues from an industrial and customer view as well. The original joint radiation hardened microelectronics S&T strategy group has developed a joint strategy and is working cooperatively with a broad range of government interests (including DOE) to effectively plan S&T investments.

Another area where joint strategies have occurred is in the planning of DARPA programs. As DARPA programs are initially developed, Service representatives frequently work very closely with DARPA program managers to develop strategies; eventually Service personnel play a role in the final execution. It is common for Service representatives to identify opportunities for DARPA and take a significant role in defining a joint strategy for DARPA investments. It should be noted though that this process is not formal and cooperation is dependent upon independent initiatives of the people involved.

4.3 MILITARY-DEVELOPED MICROELECTRONICS TECHNOLOGY

The military invests in developing strategic microelectronics technology that can be then produced for use in defense systems. These investments come from three major areas:

- Service/Office of the Secretary of Defense (OSD) direct microelectronics investment
- Program office investment
- Supplier/contractor investment

In this discussion we will not discuss program office and supplier/contractor investments. Although important, program office investments are not major and do not indicate any major trend, and the supplier/contractor investments are based on profit motives and generally do not capture DOD strategic issues. For the most part, program office and supplier/contractor investments are not coordinated with any central DOD strategy, planning, or budgetary process.

The OSD Science and Technology (S&T)[2] microelectronics investment comes from the Services (Army, Navy, Air Force), the Defense Special Weapons Agency (DSWA), the Ballistic Missile Defense Office (BMDO), and OSD's Defense Advanced Research Projects Agency (DARPA). Each Service has specific budgetary lines of funding for basic research (DOD Category 6.1), technology development (Category 6.2), and technology demonstrations (Category 6.3). Each category is discussed in further detail in the following subsections.

4.3.1 Microelectronics Basic Research (Category 6.1)

DOD basic research is focused on the physics and chemistry of microelectronics devices and the development of innovative devices and circuits. Much of the work is involved with gaining a deeper understanding of how microelectronics devices work as features shrink and, most importantly, to understand the behavior of the great variety of devices that can be engineered with semiconductor materials. Understanding behavior in many of these complex devices involves not only understanding simple transport mechanisms but also chemical, thermal, mechanical, and, today, quantum behavior as well.

Basic research is performed using several different strategies. There is a large portion of basic research that is performed in academic institutions and, for the most part, is loosely guided by defense requirements. The Services and OSD make basic research investments at universities. Most of the Services have a separate university research budget and planning authority. DARPA's university investments are integrated with their programs.

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[2] S&T investments refer to all investments in categories 6.1, 6.2 and 6.3, covering basic research through the demonstration of the technology.

The remaining Service basic research investments are made under a wider basic research planning authority which considers larger, overall topics than just microelectronics. Basic research is performed not only in universities, but in the Service labs, industry, and at several DOE laboratories.

4.3.2 Microelectronics Technology Development (Category 6.2)

DOD technology development is focused on taking the understanding and control of microelectronics behavior gained in the basic research and actually building interesting devices. Each Service has a specific budget and planning authority for technology development. Technology development are also spread over universities, Service labs, and industry and DOE labs, but significantly less investment is made in universities, as the goal is to start building devices of specific military interest.

4.3.3 Microelectronics Technology Demonstration (Category 6.3)

DOD investments are made to specifically transition a new technology into availability and use. This is a particular challenge since most microelectronics innovations have to be transitioned into the industrial base. Each Service and OSD make investments in technology demonstrations in order to achieve transition goals.

4.4 DOD MICROELECTRONICS PLANNING CONCLUSION

While DOD has several formal mechanisms for planning its microelectronics investment strategy, it still lacks an integrated view of DOE laboratory capabilities and resources relevant to meeting its needs. There are several reasons for this. There is only limited and informal coordination with DOE microelectronics planning and funding exercises, caused in part by a lack of centralized planning at DOE headquarters. Although DOE recently initiated an S&T strategic planning process, this is primarily a high-level reporting activity with no particular technology focus.[3] Furthermore, while some limited joint cooperative development occurs during the basic research (6.1) and technology development (6.2) phases of defense microelectronics life cycles, little, if any, joint activity takes place later on common issues of concern such as the supporting materials and equipment infrastructure and the timely insertion of microelectronics into defense systems throughout their lifetimes.

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[3] An initial database exists containing 11,000 projects in all areas.

5. SUMMARY OF RESULTS

There are a number of opportunities for DOD to utilize DOE microelectronics capabilities in support of DOD requirements. The laboratories have a wide range of microelectronics capabilities in the form of technologies and facilities relevant to DOD mission requirements.

5.1 FINDINGS

1. The DOE laboratories and facilities have significant capability in microelectronics areas outlined in the DTAP. The mapping is illustrated in Table 3.

   The mapping between a facility and a major DTAP area indicates relevant technical capability or facilities employed in S&T efforts in that particular area. The level of effort applied to a specific major area is not indicated by the mapping and may be reviewed in the specific capabilities descriptions in Appendix A for each laboratory or facility.

Table 3. DTAP Technology at Major DOE Laboratories and Facilities

Major Area	Brookhaven	Kansas City Plant	Los Alamos	Lawrence Berkeley	Lawrence Livermore	Oak Ridge	Sandia
Microelectronics	X	X	X	X	X	X	X
Electronic Materials	X		X	X	X	X	X
Electronics Integration Technology		X	X		X	X	X

2. DOE prototype production facilities in DTAP microelectronics-related areas are illustrated in Table 4. Some DOE prototype production is done for internal laboratory requirements and some for defense programs.

Table 4. DTAP-Related Prototype Production Capabilities of Major DOE Facilities

Major Area	Brookhaven	Kansas City Plant	Los Alamos	Lawrence Berkeley	Lawrence Livermore	Oak Ridge	Sandia
Microelectronics		X			X		X
Electronic Materials			X			X	X
Electronics Integration Technology		X	X		X	X	X

3. Specific technological capabilities of the DOE laboratories and facilities compared to electronics sub-areas of the DTAP are provided in Table 5. The mapping indicates significant capability without specifying the absolute level of effort.

Table 5. DTAP Technologies of Major DOE Facilities

Areas and Sub-Areas	Brookhaven	Kansas City Plant	Los Alamos	Lawrence Berkeley	Lawrence Livermore	Oak Ridge	Sandia
Microelectronics							
Mainstream Silicon Technology	X			X	X	X	X
Expanded Performance Processes, Devices and Circuits		X	X			X[a]	X
Microelectromechanical Systems	X			X	X		X
Electronic Materials							
Chemical Synthesis			X				X
Bulk and Thin Film/ nanostructure Materials Fabrication	X		X		X	X	X
Development of Materials Fabrication Processes	X		X	X	X		X
Electrical, Optical, Structural, Morphological, and Chemical Characterization	X		X	X	X	X	X
Electronics Integration Technology							
Design, Test, and Quality Assurance		X	X		X	X	X
Packaging, Interconnect, and Assembly		X	X		X	X	X
Power			X				

a. Provides fabless design, i.e., uses best outsource capability available.

5.2 OBSERVATIONS

While collecting data on capabilities and visiting facilities, information on how DOE and DOD actually manage, coordinate and perform microelectronics technology work started to emerge. The following observations highlight what was found during this study.

1. DOE does not have a centralized headquarters planning functions for microelectronics.
2. DOE recently initiated an S&T strategic planning process. Primarily, it is a high-level reporting activity, but it lacks specific microelectronics technology focus. The initial DOE database contains approximately 11,000 projects in all technology areas.
3. There is limited, informal coordination between DOE and DOD microelectronics R&D and life cycle planning and funding processes.
4. DOD lacks an integrated view of DOE laboratory capabilities and resources relevant to DOD microelectronics requirements. There have been some recent steps taken to enhance working level coordination[1], but these steps have been in technical areas where DOD was already aware of DOE laboratory capabilities. DOD has not generally considered the DOE laboratories as a source of microelectronics technology, at times delaying access to key miniaturization and reliability improvement technologies
5. DOD microelectronics planning has formal mechanisms for conducting planning and reporting among the three Services, the Defense Special Weapons Agency, the Defense Advanced Research Projects Agency, and Ballistic Missile Defense Office. DOE has no such mechanisms.
6. DOD does not participate in the SEMATECH microelectronics project database, contributing to an incomplete view of government and industry microelectronics investments. By not participating in this project, DOD is unable to

[1] Recent steps include DOE becoming a member of DOD's Rad-Hard Oversight Committee (RHOC) being formed as a result of the recent Rad-Hard Integrated Product Team (IPT). The RHOC is expected to coordinate technology development as well as procurements across government microelectronics. DARPA is actively funding programs to commercialize Sandia's unique I-MEMS technology. Cooperative MEMS programs have been formalized between Sandia and the Air Force Laboratory (formerly the Phillips Laboratory) under a DOD-DOE Memorandum of Understanding (MOU).

benefit from the planning information provided by DOE and commercial industry in this database.

5.3 CONCLUSION AND RECOMMENDATIONS

As a result of our preliminary analysis, we concluded that a number of opportunities exist for cooperative activities in microelectronics.

To take advantage of these opportunities DOD should consider the following:

1. Explore DOE laboratory capabilities for relevant S&T efforts as well as prototype production of unique defense electronics.
2. Identify mechanisms to increase involvement in joint DOD and DOE microelectronics planning and investment.
3. Be specifically involved in major DOE efforts in electronic materials, lithography and related manufacturing processes, radiation hardness, and electronic integration technologies (e.g., multi-chip modules).

APPENDIX A. MICROELECTRONICS CAPABILITIES OF DOE FACILITIES

This appendix summarizes information from various sources to describe the microelectronics capabilities at each DOE laboratory and facility.[1] Each description begins with a chart of contact, budget, and overall staff information[2]. The chart is followed by a summary of work, if any, that is relevant to microelectronics. These summaries are presented by DTAP category to facilitate the correlation of DOE microelectronics capabilities with DOD microelectronics needs.

Based on preliminary analysis of databases and other relevant information, the IDA study team made site visits to selected DOE laboratories and facilities. Of the 39 DOE sites, IDA visited the following:

1. Brookhaven National Laboratory,
2. Kansas City Plant,
3. Lawrence Berkeley National Laboratory,
4. Lawrence Livermore National Laboratory,
5. Los Alamos National Laboratory,
6. Oak Ridge National Laboratory, and
7. Sandia National Laboratory.

The descriptions for these sites are much more comprehensive than sites not visited. Only sites where microelectronic activity was identified are included in this appendix.

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[1] Many of the descriptions have been taken with permission from the Mid-Atlantic Technology Application Center Federal Laboratories Database. Information was also obtained from laboratory Internet world wide web sites, as well as from published and non-published briefing materials provided by the laboratories.

[2] Budget and staff information are given for the entire laboratory. Contact information is for the microelectronics area specifically.

A.1 AMES LABORATORY[3]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	AMES Laboratory 311 TASF Iowa State University Ames, IA 50011-3020 United States
Contact:	Robert S. Harris
Phone/Fax:	Phone: (515) 294-2635 Fax: (515) 294-3751
BBS/Internet:	harris@ameslab.gov
Director:	Dr. Thomas J. Barton
Budget:	$33 million (FY94)
Employees: Professional: 400 Other: 200 Total: 600	Percent Effort: R&D: 90% Testing: 5% Other: 5%
Contractor:	Iowa State University
Type of Operation:	Government owned and contractor operated

Ames Laboratory conducts basic and applied research to advance the understanding of chemical, engineering, materials, mathematical and physical sciences that underlie energy technologies, as well as other technologies essential to national interests.

For example, the Materials Chemistry Program is diverse in scope, scientists in this program focus on the design, synthesis and study of new materials with unique properties of potential value to American technology, new or improved routes to materials of demonstrated strategic and/or economic importance, and detailed studies to gain fundamental understanding for the structure and chemistry of important materials to control both beneficial and deleterious properties. In the Chemical Structures group,

[3] Some of the material for this section was taken from the AMES web site, http://www.ameslab.gov.

scientists focus on the synthesis of entirely new types of compounds so that potentially useful new materials may be recognized and available. A major goal of the Polymer and Engineering Chemistry Task is the development of synthetic routes to a wide variety of silicon carbide and silicon nitride polymers and their application as convenient thermal precursors to Si-C and Si-N fibers. High Temperature and Surface Chemistry emphasis includes detailed studies of surface lubrication, corrosion, electrocatalysis, and a new initiative, quasicrystals. Ultimately, these studies should aid in designing more stable and efficient coatings or additives for application as lubricants. A materials scientist has also created the first non-carbon example of buckyballs, which opens up pathways to new materials and valuable insights into the way compounds form.

A.1.1 Electronic Materials

Internationally recognized for preparing ultra high-purity and well-characterized metals, alloys, composites and single crystals, Ames Laboratory is now focusing research on the design, synthesis, and processing of new nontraditional materials such as organic polymers and organometallic materials to serve as novel semiconductors, processable pre-ceramics, and nonlinear optical systems.

A.2 ARGONNE NATIONAL LABORATORY[4]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Industrial Technology Development Center 9700 South Cass Avenue MS ITD-900 Argonne, IL 60439-4832 United States
Contact:	Paul Eichamer
Phone/Fax:	Phone: (630) 252-9771 Fax: (630) 252-5230
BBS/Internet:	pdeichamer@anl.gov
Director:	Dr. Alan Schriesheim
Budget:	$614 million (FY94)
Employees: Professional: 2,000 Other: 2,800 Total: 4,800	Percent Effort: R&D: 100% Testing: Other:
Contractor:	University of Chicago
Type of Operation:	Government owned and contractor operated

Argonne National Laboratory (ANL) is a "multiprogram" laboratory, which for industry translates into broad applicable technology relating to the use of advanced materials and manufacturing processes, advanced sensors, and modeling, simulation, and high performance computing capabilities.

A.2.1 Electronic Materials

The electronic materials program at ANL includes applications of synchrotron radiation to the characterization of materials. This program is using national synchrotron radiation facilities for the study of structures and electronic properties of materials. It will

[4] Some of the material for this section was taken from the Argonne National Laboratory web site, http://www.anl.gov/LabDB/progcapform.html.

play the leading role at the Basic Energy Sciences Synchrotron Radiation Center, and will be constructed at the 7 GeV Advanced Photon Source. This research group operates several x-ray scattering beam lines at the National Synchrotron Light Source (NSLS), and one beam line at the University of Wisconsin's Synchrotron Radiation Center. The group has also developed in-house rotating anode facilities used for single crystal and powder diffraction measurements. Research interests are broad, including the studies of surfaces and interfaces, studies of the electronic properties of materials, and time-dependent studies. The time-dependent studies will receive special emphasis at the Advanced Photon Source[5], where real-time measurements at nanosecond time scales will be possible.

[5] For more information, see the Argonne National Laboratory Web site, http://www.anl.gov/LabDB/progcapform.html, or contact the Industry Liaison, Industrial Technology Development Center, Bldg. 900, Argonne National Laboratory, 9700 S. Cass Ave., Argonne, IL 60439.

A.3 BROOKHAVEN NATIONAL LABORATORY

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Office of Technology Transfer P. O. Box 5000 Building 475-D Upton, NY 11973-5000 United States
Contact:	Margaret C. Bogosian
Phone/Fax:	Phone: (516) 344-7338 Fax: (516) 344-3729
BBS/Internet:	dorryt@magadd2.nov.add.bnl.gov
Director:	Dr. Peter Bond
Budget:	$408 million (FY94)
Employees: Professional: 1,243 Other: 2,106 Total: 3,349	Percent Effort: R&D: 95% Testing: Other: 5%
Contractor:	Associated Universities
Type of Operation:	Government owned and contractor operated

Brookhaven National Laboratory (BNL) carries out basic and applied research in the physical, biomedical, and environmental sciences, and in selected energy technologies. BNL performs microelectronics work in its National Synchrotron Light Source (NSLS) Department and its Instrumentation Division.

BNL's NSLS is the world's largest facility dedicated to the production of synchrotron light. Over the course of a single year, nearly 2,300 researchers representing more than 350 institutions (over 50 of them corporations) work on projects that range from developing an x-ray microscope to studying the surfaces of various materials. For example, in partnership with Grumman Aerospace Corporation and its subcontractor, General Dynamics, BNL has taken the lead in a national effort to design a prototype production facility for the manufacture of the next generation of computer chips. The

compact synchrotron facility would use a new and promising technique called *x-ray lithography.* IBM made the first test chips using this technique on its beam line at the NSLS.

BNL's Instrumentation Division has several small, research-scale efforts in the microelectronics area involving one or two scientists for each of the following efforts: hybrid and monocircuit design and test; data acquisition system design; silicon detector design, fabrication, and test; and silicon micromachining. In supporting these efforts, BNL has a small clean room for detector fabrication, a printed circuit shop, and a machine shop. Specific Instrumentation Division facilities include:

1. Gas Detector Laboratory (clean rooms, fabrication, X-ray source and test facilities);
2. Semiconductor Detector Laboratory (clean rooms, oxidation, mask alignment, wire bonding);
3. Hybrid Circuits Laboratory (low noise electronics prototype development);
4. Monolithic Circuits Laboratory (design, simulation, testing);
5. Computer Aided Circuit Layout (design of detector electrodes and electronics boards, up to 12 layers);
6. Multi-layer Printed Circuits (fabrication of detector electrodes, 12 layer circuit boards);
7. Optics and Metrology Laboratory (digital optical profiler, long trace profiler);
8. Laser Laboratory (photo-emission and fast switching studies, electro-optic modulator testing);
9. Electron Microscopy Laboratory (fabrication of microstructures, analytical microscopy);
10. Vacuum Deposition Laboratory (coatings and multi-layers); and
11. Solid State Irradiation Facility (SSIF) (a 20 kCi cobalt source).

A.3.1 Microelectronics (Mainstream Silicon Technology)[6]

The NSLS Department operates an X-Ray Ring and a VUV (vacuum ultra violet) Ring. X-ray, ultraviolet, and infrared (IR) radiation from the storage rings is guided into over 83 beamlines, or experimental stations, where it is used in many fields of research. Approximately 50 of the beamlines are dedicated to materials related to microelectronics, with four of the beamlines performing lithography. An example of the available beamlines is shown in Table A-1. The facility operates throughout the year, and time on a beamline can be obtained.

NSLS beamlines support a variety of physics studies related to microelectronics and electro-optics. One such beamline has been used for a research program in Extended X-ray absorption fine structure spectroscopy (EXAFS), Surface EXAFS (SEXAFS), and Near-edge EXAFS (NEXAFS). The main effort is to characterize electronic and electro-optic materials constituent atoms at very low densities and determine geometric distribution within the material. SEXAFS looks at surface constituents and impurities. NEXAFS provides chemical information through chemical binding related shifts in electronic absorption levels. Shifts as small as 7 to 8 volts have been detected.

Other groups have used other rings and beamlines to perform lithography experiments constructing 0.1 μm features on silicon with reflective X-ray feature masks. These experiments are described as extended ultra-violet (EUV) lithography. This work is based on 13 nm wavelength photons. Research in lithography down to 50 nm features has been performed and is estimated to be somewhere near the smallest size for practical Field Effect Transistor (FET) transistors in silicon.

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[6] Some of the material for this section was taken from the Brookhaven National Laboratory web site, the NSLS introduction, http://www.nsls.bnl.gov/Intro/IntroMenu.html.

Table A-1. An Example of a NSLS Beamline

Energy Range (KeV)	Crystal Type	Resolution @Ec (deltaE/E)	Flux (photons/sec)	Spot Size focused (mm)	Total Horizontal Angular Acceptance (mradians)
1.5 - 15	Si(111)	2×10^{-4}	2×10^{11} @ 5 KeV (100mA, 2.5 GeV)	-1H x 1V @ less than 3 KeV	5
4.5 - 26	Si(111)	2×10^{-4}	5×10^{8} @ 10 KeV (100mA, 2.5 GeV)	10H x 0.5V -unfocused	0.5
8 - 35	Si(311)	2×10^{-4}	5×10^{8} @ 25 KeV (100mA, 2.5 GeV)	10H x 0.5V -unfocused	0.5

Other Mainstream Microelectronics Efforts

BNL's Instrumentation Division uses CMOS technology to make integrated front-end circuits for various types of radiation sensors, including:

1. Low noise charge-sensitive preamplifiers
2. Pulse shaping active filters
3. Flash analog-to-digital converters
4. Precision, on-chip calibration circuits
5. Timing discriminators
6. Analog multiplexers

A.3.2 Microelectronics (MEMS)[7]

In recent years the technique of LIGA, a German acronym which translates to X-Ray Lithography, Electroplating, and Plastic Molding, has emerged as the cutting edge technology in the manufacture of small, high-precision mechanical devices. At the NSLS, the X-Ray Ring provides a unique opportunity for the utilization of hard X-rays to extend high precision manufacturing using lithographic techniques to length scales on the order of centimeters. Conventional LIGA techniques typically yield structures less than 500 mm thick. The deep penetration of hard X-rays in the resist provides the additional opportunity to fabricate true 3-D objects with re-entrant geometries, in contrast to the 2-D structures typical of standard LIGA techniques. A research program is currently being developed on beamline X27B.

Micromachining at the NSLS[8]

In 1988, researchers in Germany and the United States began to investigate using the techniques developed for semiconductor device fabrication to make very small mechanical components. In the few years tremendous progress has been made. The group in Germany was so optimistic about the future of this new technology that they created a commercial venture, Microparts, to exploit it. In the United States relatively little enthusiasm was generated outside the research groups directly involved.

Part of the reluctance of industry to take the process seriously is that until now, it has been essentially a two-dimensional technology. Typical structure heights in semiconductor devices are less than 1 micrometer. The semiconductor process uses visible light to irradiate a polymer resist over a silicon wafer through an patterned opaque mask. The irradiated part of the layer can then be dissolved away by a solvent, leaving the non-irradiated part intact. Subsequent diffusing or coating transfers this pattern onto the silicon. The micro-machining process adds one more step to this procedure. It uses electro-deposition to form metal parts in the holes left in the resist. In effect, the resist material is made into a mold for forming microstructures. This process has limited application for the manufacture of moving parts since the structures are only as thick as the depth of the holes in the resist. To make deeper holes and hence thicker components, it would be necessary to

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[7] Some of the material for this section was taken from the Brookhaven NSLS web site, Micromachining at the NSLS, http://suntid.bnl.gov:8080/nslsnews/0394/a07.html.

[8] Material for this section was taken from Brookhaven NSLS web site, Micromachining at the NSLS, http://suntid.bnl.gov:8080/nslsnews/0394/a07.html.

irradiate several millimeters down into a resist. A variety of test objects have been produced at the NSLS.

The use of soft x-ray lithography was the breakthrough which so excited the German group, since it made structures possible with heights up to 50 micrometers. Using this technology, both the United States and Germany developed novel micromechanical devices. Micro-turbines, stepping-motors, spectrometers, IR filters, spinarette nozzles are just a few examples of research products. However, there were still serious limitations on what could be built using 50 micrometer thick objects. A method for creating even thicker objects was needed.

The solution to this problem is being provided by the NSLS X-Ray Ring, which produces a large flux of hard x-rays. These hard x-rays can penetrate many millimeters of the polymer material used to define components. Unfortunately, the hard x-rays also pass easily through conventional mask structures. Thus, a highly absorbing mask must first be fabricated using previously developed soft x-ray techniques. It is then possible to take the final step in the development of a truly three-dimensional micro-machining technology. In collaboration with one of the world's leading research teams in this field, that of Prof. H. Guckel at the University of Wisconsin, Madison, NSLS staff has begun to develop the instrumentation and materials necessary to begin manufacturing these thick microstructures at Brookhaven. Significant results have already been achieved and development is proceeding at a rapid pace. Pins as small as 50 micrometers in diameter have been made whose diameters are uniform to better than 1 micrometer over their full 3 mm length. More complex three-dimensional structures are also possible. It is hoped that other researchers will be able to make use of the facilities being developed at NSLS in the near future.

A.4 KANSAS CITY PLANT[9]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	AlliedSignal Federal Manufacturing & Technologies D/200, MS 1D40 P. O. Box 419159 Kansas City, MO 64141-6159 United States
Contact:	Dennis Stittsworth
Phone/Fax:	Phone: (816) 997-4596 Fax: (816) 997-2536
BBS/Internet:	www.kcp.com
Director:	Karen Clegg
Budget:	$350.8 million (FY96)
Employees: Professional: Other: Total: 3,435	Percent Effort: R&D: Testing: Other:
Contractor:	AlliedSignal Aerospace
Type of Operation:	Government owned and contractor operated

The Kansas City Plant (KCP) is a DOE manufacturing facility operated by AlliedSignal Aerospace. KCP has the mission assignment from DOE to manufacture microelectronic devices and has consistently provided high quality and high reliability weapon system microelectronic devices since the late 1960's. KCP's microelectronic devices are fabricated in 13,000 square feet of state-of-the-art Class 100 and Class 10,000 cleanrooms. The KCP production facility can produce medium-scale production quantities of up to hundreds per month of individual part numbers. Capabilities have been established to design, fabricate, and test hybrid microcircuits and multichip modules

[9] The Kansas City area office of DOE provided the following description which is incorporated in its entirety.

(MCMs) and to package semiconductor devices. These RF, digital, and analog microelectronic devices have been utilized in products such as radars, firesets, programmers, and secure systems where miniaturization and high reliability electronic packaging are required.

A.4.1 Electronics Integration Technology

KCP's microelectronic capability was developed to keep pace with weapon requirements of reduced package size, increased frequency, increased circuit density, and improved reliability. These needs have been met with a wide range of microelectronic capabilities that include thin film metallization (500 angstroms to 10 μm), thick film metallization (12 to 18 μm), precision thin film resistors, close tolerance ceramic machining for *via* holes, and various types of substrates such as alumina, fused silica, and aluminum nitride. KCP has the ability to fabricate RF and logic hybrid microcircuits and MCMs utilizing a wide variety of substrates, semiconductor die, applique components, and intraconnection methods.

Assembly techniques required to support microelectronic fabrication have been developed, including automated gold and aluminum wire bonding, epoxy and eutectic semiconductor die attach, hermetic package sealing, and microcircuit preconditioning. Extensive test equipment design and fabrication support is available to provide electrical testing capability. Design flexibility is maintained through computer simulations that include electrical (RF, digital, analog), mechanical, and thermal properties. Manufacturing flexibility is maintained through a wide variety of process capabilities that are characterized and statistically controlled.

A number of new microelectronic technologies are being driven by design requirements to package new and more electronic functionality into smaller volumes. Some of these product requirements include the use of optical triggering systems, high frequency RF devices in the range of 20-100 GHz, large semiconductor chips with increased I/0 requirements and 70 μm pitch bonding pads, and high thermal dissipation requirements. Transmitter/Receiver (T/R) modules which contain the logic and RF functions in a single package are using high speed gallium arsenide (GaAs) monolithic microwave integrated circuits (MMICs) mounted to the substrates. High speed, high density MCMs are being used in digital applications that require clock frequencies up to 800 MHz. KCP has also developed complete hybrid microcircuit assembly and semiconductor packaging capabilities to manufacture complex microcircuits for nuclear

weapon requirements in excess of military standard space class "S". As described in Table A-2, KCP is focused on developing new technologies required for their mission area.

Table A-2. Kansas City Plant New Technology Capabilities

Process/Product Area	New Technology
Metallization and Films	Thin film capacitors (polyimide, Ta_2O_3)
	Thin film high voltage capacitors with special dielectric
	Thin film air bridges
	Precision thin film patterns with sub-mil features
	Thin film slapper detonators
	Thin film high voltage switches
	Photosensitive polyimide coating
	Pattern copper plating
	Thick film high voltage capacitors
	Thick film sensors
Substrates	Diamond substrates
	Aluminum nitride substrates
	Excimer laser machining
Semiconductor device attachment	Fluxless solder attachment
	Flip chip bonding
	Bumping of devices
	70 µm pitch wire bonding
	Ball grid arrays

A.5 LAWRENCE BERKELEY NATIONAL LABORATORY[10]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Technology Transfer Office 1 Cyclotron Road MS 90-1070 Berkeley, CA 94720 United States
Contact:	Cheryl Fragiadakias
Phone/Fax:	Phone: (510) 486-7020 Fax: (510) 486-6457
BBS/Internet:	cafragiadakis@lbl.gov
Director:	Dr. Charles V. Shank
Budget:	$282 million (FY94)
Employees: Professional: 1,620 Other: 1,823 Total: 3,443	Percent Effort: R&D:100% Testing: Other:
Contractor:	University of California
Type of Operation:	Government owned and contractor operated

Lawrence Berkeley National Laboratory (LBNL) conducts general science research in many areas (e.g., accelerator and fusion research, nuclear science, physics, material and chemical sciences). LBNL has strengths that are relevant to microelectronics in lithography, materials and bulk processes, interconnects, and process integration. Specific research programs focus on ion sources for heavy-ion and magnetic fusion, x-ray optics, advanced metallic and ceramic materials, electron microscopy of crystal defects, superconductivity, and atomic physics.

[10] Some of the material for this section was taken from the Lawrence Berkeley Internet world wide web site, http://www.lbl.gov.

A.5.1 Microelectronics (Mainstream Silicon Technology)

LBNL's Advanced Light Source (ALS) is a third-generation synchrotron that has been optimized to produce the highest brightness source of soft x-ray and vacuum ultraviolet photons. ALS features a family of spectral microscopies and other imaging capabilities (e.g., interfaces between interconnect materials, interfacial chemistry of layered structures susceptible to delamination, and submicrometer characterization of contaminants on wafer surfaces). LBNL also maintains a nano-fabrication facility (e.g., 100 kV e-beam writing a 2.5 nm spot with a 65 μm field), EUV lithography capabilities (13 nm metrology of aspheric multilayer optics in support of the national program for sub 100 nm devices), and non-lithographic patterning and electronics capabilities in novel electronic nanostructures.

A.5.2 Microelectronics (MEMS)

The Center for X-Ray Optics (CXRO) has developed integrated capability in deep-etch x-ray lithography that includes the fabrication of suitable x-ray masks and electoplating of thick, high aspect ratio microstructures. CXRO has developed a new x-ray mask fabrication technology based on a class of thick photoresists developed for the magnetic thin-film head market. This technology allows the use of standard photolithography to pattern the thick (30 μm) gold absorbers necessary for LIGA masks.

The LIGA microfabrication process involves using deep etch x-ray lithography along with electro-forming to produce a metal part or mold of high aspect ratio. Collimated (parallel) x-ray light from the ALS is being used to develop the LIGA process. This new fabrication capability will be integrated with expertise in finite element analysis and design of precision parts. Other methods of microfabrication have been limited to parts with thicknesses less than 0.5 mm. The LIGA process will make it possible to produce very precise parts with a thickness greater than 1 mm. Potential applications include high density magnetic storage devices, precision bearings and bushings for the aerospace and automotive industries, flow controllers, and biological microfilters.

A.5.3 Electronic Materials

The Materials Science Division performs research in x-ray diffraction, spectroscopy, proton induced x-ray emission, and ion scattering. LBNL's electronic materials group has complete semiconductor characterization, processing, and fabrication capabilities to produce infrared and x-ray sensors using germanium, silicon, gallium

arsenide, indium phosphide, and zinc selenide. This group has capabilities in the areas of crystal cutting, lapping and polishing, chemical etching, ion implantation, thin-film deposition and microfabrication techniques. Special semiconductor devices that have resulted from their research include: far IR extrinsic photoconductors covering 50-250 μm; heavily doped Ge thermistors for bolometers operating from 1 K to 20 mK; x-ray and gamma-ray p-i-n junction detectors for a wide range of accelerator, physics, and x-ray synchrotron applications; and high energy physics vertex detector arrays.

The National Center for Electron Microscopy (NCEM) is one of the nation's primary research facilities for the use of high voltage electron microscopes in the examination of atomic structure of materials. NCEM has four unique facilities:

1. A 1 MeV JEOL Atomic Resolution Microscope (ARM) used to examine grain boundaries or interface structures.
2. A 1.5 MeV Kratos HVEM with the highest accelerating voltage available in the U.S. for dynamic in-situ studies.
3. A computer image analysis, processing and simulation facility to relate the images to atomic positions with high precision.
4. An Analytical Electron Microscope (AEM) with spectrometers to examine the chemical composition of nanometer-sized regions on a specimen.

A.6 LAWRENCE LIVERMORE NATIONAL LABORATORY[11]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Technology Transfer P. O. Box 808 L-795 Livermore, CA 94551 United States
Contact:	Technology Transfer Outreach
Phone/Fax:	(510) 423-5660 / (510) 423-8988
BBS/Internet:	techtrans@llnl.gov / http://www.llnl.gov
Director:	John Nuckolls
Budget:	$950 Million
Employees: Professional: 4557 Other: 2762 Total: 7319	Percent Effort: R&D:100% Testing: Other:
Contractor:	University of California
Type of Operation:	Government Owned And Contractor Operated

Lawrence Livermore National Laboratory (LLNL) provides scientific and technological tools needed to meet critical national missions in three areas: global security, global ecology, and bioscience. The global security program focuses on reducing nuclear danger by ensuring the safety, security, and performance of U.S. weapons. The program also focuses on preventing and countering nuclear proliferation by applying expertise in nuclear science and technology. LLNL is also applying their capabilities to meeting the DOD need for conventional, high-technology weapons.

Activities in microelectronics and optoelectronics at LLNL are coordinated by the Center for Microelectronics and Optoelectronics (CMO). CMO is the umbrella organization for several LLNL activities in materials theory, modeling, and simulation;

[11] Some of the material in this section was taken from the Lawrence Livermore National Laboratory Web site, http://www.llnl.gov/.

materials research development; characterization and modeling of fundamental material properties; and thin-film processing and microfabrication technology. There are application programs in semiconductors processing and process modeling, lithography, electronic packaging, communication and computing systems, magnetic storage, and flat panel display technologies. LLNL's strengths in microelectronics and optoelectronics arise from high-speed detection, transmission, and transient recording requirements of the nuclear test program, and from diagnostic and fabrication requirements of the inertial confinement (laser) fusion program.

A.6.1 Microelectronics (Mainstream Silicon Technology)

LLNL has over 12,000 square feet of Class 10-100 clean rooms housing fabrication equipment for silicon processing and micromachining, III-V semiconductor applications, optoelectronics, guided wave photonics, and IC packaging. LLNL has extensive facilities (30,000 square feet) for materials characterization. For example, routine and advanced x-ray facilities include a fully instrumented rotating target source for crystal structure determinations. An extensive array of modern electron beam instruments are also available. Micro structures and micro structural evolution are studied with state-of-the-art atomic force and scanning tunneling microscopy, while interface science is greatly enabled by the development of a unique bicrystal fabrication facility.

Semiconductor Processing

LLNL has begun work under a Cooperative Research and Development Agreement (CRADA) to develop fundamental scientific knowledge that will lead to improved performance in microelectronic devices. The project takes advantage of the breakthrough capabilities developed at LLNL in the area of advanced molecular dynamics simulations and the experimental capabilities to study supersonic molecular and reactive ion-beam-induced modifications of surfaces that have been developed by industry partners.

LLNL has developed a new doping process for the formation of shallow junctions, Gas Immersion Laser Doping (GILD), which is compatible with sub-0.2 μm feature sizes that cannot be fabricated using ion implantation. LLNL is developing a projection version of GILD, under funding from DARPA and SEMATECH, that could be integrated easily into both conventional and flexible fabrication facilities.

Interconnects

LLNL is developing a copper electroplating process under Intel and SEMATECH funding that provides void-free vias and embedded metal traces while reducing equipment cost. LLNL has extensive experience in low dielectric constant materials such as polymer and silica and other inorganic oxides gels and foams. The use of finite element codes to model thermal and mechanical properties of materials has been a specialty of the LLNL core technologies.

Equipment design and modeling

Plasma experiments and plasma modeling at LLNL are core technologies deriving from the inertial confinement fusion and nuclear weapons design and effects programs. A charged-particle transport, chemistry, and particle generation code is being developed under CRADA agreements among IBM, AT&T, and LLNL to model plasma etching tools and to validate these tools on state-of-the-art equipment. LLNL is studying scaling issues for plasma processing of 300 to 400 mm silicon wafers. LLNL is developing plasma diagnostics to provide the cheap and reliable sensors needed to make an impact on the fabrication floor. An improved plasma control technology is under development.

Lithography

In extreme UV lithography, LLNL is actively collaborating with two other national laboratories and nine industrial partners (AT&T, Intel, Ultratech Stepper, AMD, KLA, Jamar Technology, Micrion, Tropel, Hoya USA). The goal of the project is to provide U.S. industry with a capability for cost effective production of advanced, high density ICs with feature sizes as small as 0.1 μm. LLNL's specific contributions to the collaborative project include laser technology, EUV radiation production, optical design, EUV mirror technology, reflective mask technology, and advanced metrology of high precision optics. LLNL is playing a major role in point source x-ray lithography by developing the laser driven source for the National Lithography Program sponsored by DARPA. LLNL has developed a unique solid state laser technology with peak powers in the range of 109 watts and average powers which will soon be at the 1 kW level.

Electron and Ion Beam Technologies

LLNL has over 100,000 square feet of facilities devoted to electron beam research and testing. These facilities house a number of state-of-the-art tools for prototype part process and development, advanced composite materials production and high rate thin

film coating. LLNL's Ion Beam Laboratory has advanced facilities with tools for ion implantations of atoms inside the surfaces of materials, and ion irradiation's for improving the adhesion of thin films.

Modeling and Simulation

LLNL has a number of modeling and simulation programs concerning microelectronics. An atomic scale 3-D simulator has been developed for accurate, predictive modeling of ion implantation and dopant diffusion in silicon. Another atomic scale 3-D simulator has been developed for metal line deposition and microstructure development. INDUCT95 is a 2-D time-dependent plasma discharge model that has applications in ion extraction at low pressure for laser induced plasmas and in glow discharges for flat panel displays. Equipment modeling has been done for plasma etching and deposition, chemical down stream etching, chemical vapor deposition, and rapid thermal processing.

A.6.2 Electronics Integration Technology

LLNL work in packaging covers electronics, optoelectronics, and modeling and simulation. In addition to extensive development of microchannel and other heatsinks, LLNL has developed new heat spreader materials for microelectronics such as diamond coatings and a copper-diamond composite substrate. LLNL has also developed manufacturable silicon microbench packaging for hybrid integration with electronics and fiber-to-waveguide alignment ease. LLNL has been developing general purpose electromagnetic (E&M) modeling tools for both time and frequency domains. LLNL is currently adapting E&M modeling tools to better study important issues in microelectronic interconnects.

A.7 LOS ALAMOS NATIONAL LABORATORY[12]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Industrial Partnership Center P. O. Box 1663, Mail Stop C 331 Los Alamos, NM 87545 United States
Contact:	Ms. Charrly Berger
Phone/Fax:	(505) 665-9090/(505) 667-4098
BBS/Internet:	cberger@lanl.gov / http://www.lanl.gov
Director:	Dr. Siegfried S. Hecker
Budget:	$1.2 Billion Fiscal Year: 1996
Employees:3373 Professional: Other: 4192 Total: 7565	Percent Effort: R&D:100% Testing: Other:
Contractor:	University of California
Type of Operation:	Government Owned And Contractor Operated

Los Alamos National Laboratory (LANL) is one of the largest multidisciplinary institutions in the world. LANL's primary mission is to provide a technical foundation to reduce global nuclear danger. As one of its eight core competencies, LANL has theory, modeling, and high-performance computing capabilities that have led to advances in materials design; to new fabrication methods for the semiconductor industry; and to new miniature, nanoscale devices capable of self-assembly.

A.7.1 Microelectronics

LANL was chosen by SEMATECH and the Semiconductor Research Corporation (SRC) to serve as a Center for Semiconductor Modeling and Simulation. The mechanism for this effort is a five year LANL-SRC Cooperative Research and Development Agreement (CRADA) that will be supported by DOE with annual support of $10 million.

[12] Some of this material was taken from the Los Alamos National Laboratory Web site, http://www.lanl.gov/.

The goal of the program is to develop an advanced suite of predictive TCAD tools for use to manufacture 0.1-0.25 μm devices. The Center for Semiconductor Modeling and Simulation derives its strengths from the multi-disciplinary materials modeling program in the Theoretical Division of LANL. From advances in materials modeling and high performance computing, design tools for bulk processing, wafer-state topological CVD, and interconnect performance and reliability are being developed and applied to next-generation microelectronics devices to substantially reduce manufacturing cost and time-to-market. Development of predictive modeling and simulation tools will substantially reduce manufacturing cost and time-to-market.

The Space Engineering Group, within the Nonproliferation and International Security Division, has a full suite of design tools to perform systems engineering and detail design of ASICs (e.g., analog, digital, bipolar, CMOS, GaAs, and radiation hardened). Work in microsensors is also occurring, with development of silicon sensors for photon and particles, diamond sensors, and IR detectors. Another Space Engineering Group project is to develop 2010 Priority Technologies (e.g., ULSICs, high density packaging, and ultra high speed and low power devices). Unique custom CAD design development software developed at LANL dramatically reduces non-recurring engineering costs associated with ASIC and MCM development.

The LANL Physics Division has in-house microelectronics fabrication, parameter extraction, and test capabilities. The Physics Division can characterize electronic and electro-optic components from DC to 50 GHz in the frequency and time domains. They also design analog ICs, and then package many of them as hybrid MCM circuits. Thick film, thin film, and TOS processes are available.

A.7.2 Electronic Materials

Over the past five decades, LANL materials researchers have contributed to a host of programs relating to national defense, energy, space, environment, transportation, and biotechnology. LANL has synthesis, processing, fabrication, characterization, imaging, and modeling capabilities that support microelectronics.

LANL is synthesizing materials that will function under extreme conditions or unusual applications. Such materials include ceramics that retain their strength at extremely high temperatures and amorphous metal alloys that can be extruded like plastic. LANL is also developing materials for exotic applications, including some polymers that emit light and others that store huge amounts of electrical charge. LANL advances in

plasma science applications based on work in plasma ion implantation, etching, and deposition facilitate new, environmentally conscious approaches to manufacturing and surface modification of materials with wide industrial applications.

The Materials Science and Technology Division, Chemical Science and Technologies, and Theoretical Divisions have groups that focus on novel materials for application in "electronic" devices including organic light emitting polymers, organic transistors, fuel cells, supercapacitors, chemical sensors, microwave devices, high temperature superconducting devices, and electrochemical reactors.

A.8 OAK RIDGE NATIONAL LABORATORY[13]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	P. O. Box 2008 MS 6266, 4500 N Oak Ridge, TN 37831 United States
Contact:	Mr. Joe Culver
Phone/Fax:	Phone: (423) 576-0235 Fax: (423) 574-0595
BBS/Internet:	culverjw@orn.gov
Director:	Dr. Alvin Trivelpiece
Budget:	$577 million (FY94)
Employees: Professional: 2,633 Other: 2,406 Total: 5,039	Percent Effort: R&D: 75% Testing: Other: 25%
Contractor:	Martin Marietta Energy Systems, Inc.
Type of Operation:	Government owned and contractor operated

The Oak Ridge National Laboratory (ORNL) primarily supports the fission nuclear fuel cycle and development of magnetic fusion energy through scientific research and technology. Primary program areas are basic energy sciences, fusion energy, fission energy development, conservation and renewable energy, defense programs, and the biomedical and environmental sciences. ORNL has three divisions working in microelectronics and related areas: the Instrument Control Division, the Solid State Division, and the Metals and Ceramic Division. ORNL has worked for all branches of the DOD, and has project management capability to do multi-million dollar efforts.

[13] This material is taken from the Oak Ridge National Laboratory world wide web site, http://www.ornl.gov.

A.8.1 Microelectronics (Mainstream Silicon Technology)

The Instrumentation and Controls Division has over 100 electronics R&D engineers, in-house prototype fabrication facilities, state-of-the-art synthesis and simulation tools and the capability to rapidly prototype ASICs and other electronic systems. The division's electronics activities include analog electronics, radiation hardened electronic systems, high temperature electronics, ASICs, electronic packaging, digital and mixed analog/digital electronics, sensors/electronics integration, radio frequency through microwave frequency, and photonics (e.g., electroptics/optical ASICs).

ORNL's primary microelectronics research is in three areas: ASICs, digital and embedded controller systems, and RF and microwave systems. The ASICs group designs about 40 ASIC chips per year, covering digital, analog, and mixed signal systems. All fabrication is outsourced. Specific emphasis has been placed on analog circuit development, where ORNL has had significant success in high-performance analog and mixed-signal chips. The digital and embedded controller systems group uses primarily off-the-shelf components, and has specific software expertise in embedded controller applications. The RF and microwave systems group specializes in non-destructive evaluation using microwave techniques, in materials processing (e.g., composites) using microwave techniques, and in niche communication systems (e.g., data communications in and out of highly reflective environments). In recent years, ORNL has developed an expertise in micro-telemetry systems (i.e., small transmitters and single-chip transmitters with integrated antennas).

A.8.2 Electronic Materials

ORNL's program in materials R&D covers the full spectrum from materials synthesis, processing, and characterization through modeling and performance evaluation. Multidisciplinary research focuses on several important classes of materials, including ceramics and composites, metals and alloys, superconductors, and thin films.

The Solid State Division has materials related activity in several facilities. ORNL's High Flux Isotope Reactor has the highest thermal neutron flux in the world and is used to research neutron scattering. Four accelerators with UHV processing chambers and interconnecting beam lines are used for ion implantation (10 eV to 1 MeV) and ion beam analysis (e.g., RBS, NRA). Thin-film processing facilities are used for pulsed laser deposition, molecular jet deposition, and ECR plasma processing. ONRL's "Z-contrast" electron microscope is the world's highest resolution scanning transmission electron

microscope, and is used to view a material's complex atomic structure with a resolution of 1.3 angstroms and distinguish one type of atom from another. A UNI-CAT beam line is under construction to facilitate synchrotron x-ray research. Finally, ONRL's Solid State Division has access to the Intel Paragon XPS-150 (one of world's most powerful computers) to research computational solid state physics.

The Metals and Ceramic Division's Theory Group is one of the world's leading groups in the calculation of the electronic structure of materials. The group has developed and uses a broad arsenal of codes for treating different types and aspects of materials. Most of these techniques are based on density functional theory. Current Theory Group projects include: magnetoresistive random access memory devices, spin-dependent tunneling devices, and electron transport in nanoscale systems.

The Metals and Ceramic Division's Microscopy and Microanalytical Sciences Group focuses primarily on the characterization of materials with advanced analytical microscopy (AEM), scanning electron microscopy (SEM), atom probe field ion microscopy (APFIM), and mechanical property microprobe (MPM) techniques. Research efforts concentrate in the development of microanalytical techniques to characterize the structure, chemistry, and mechanical response of materials and on the application of these characterization techniques to a range relevant materials science problems.

A.9 SANDIA NATIONAL LABORATORIES[14]

Parent Agency:	Department of Energy
Subelement Agency:	None
Address:	Tech Transfer & Industrial Relations P. O. Box 5800, MS 1380 Albuquerque, NM 87185-1380 United States
Contact:	Olen D. Thompson
Phone/Fax:	Phone: (505) 843-4203 Fax: (505) 843-4208
BBS/Internet:	techtransfer.info@sandia.gov
Director:	Paul Robinson
Budget:	$1.304 billion (FY94)
Employees: Professional: 3,600 Other: 4,790 Total: 8,390	Percent Effort: R&D:100% Testing: Other:
Contractor:	Lockheed-Martin
Type of Operation:	Government Owned And Contractor Operated

The major function of the Sandia National Laboratory (SNL) is to design, model, validate, and integrate the production of non-nuclear components for nuclear weapons systems. As such, SNL is responsible for the complete spectrum of DOE's Defense Program electronics, and 60% of SNL's business is based on nuclear weapons requirements. SNL has expertise, experience, and programs in most semiconductor technology areas, and has facilities unmatched by any other Federal or university research entity. The major program thrusts of SNL's microelectronics effort are in the areas of Radiation Hardened ICs, Integrated MEMS (IMEMS), Compound Semiconductors, and Sensors.

[14] This material was taken from the Sandia National Laboratories world wide web site, http://www.snl.gov.

A.9.1 Electronic Materials

SNL has three major facilities that support electronic materials technology. The Center for Compound Semiconductor Technology (CCST) has extensive processing equipment and competence in solid-state physics, materials science, and crystal growth to develop the next generation of compound semiconductor electronic and optoelectronic devices. The Advanced Manufacturing Processes Laboratory has advanced prototype manufacturing facilities for hybrid microcircuits, thin films, printed circuits, ceramics, plastics, and rapid prototyping. The Advanced Materials Research Laboratory has numerous facilities that support all aspects of electronic materials from semiconductor materials to solders.

In particular, CCST has fabrication and device characterization capabilities (e.g., direct-write electron-beam lithography and advanced dry etching) that have enabled quantum electronic devices using nanometer-scale features for gates and air-bridged point contacts. The CCST pioneered the use of lattice-mismatched (strained-layer) epitaxy for bandgap engineering of electronics and optoelectronic devices and circuits. These materials have led to the highest-performance lasers and transistors available today. Related efforts at SNL include development of control systems for magnetically levitated stages of lithography equipment, and modal and vibrational analysis of lithography equipment. SNL is working with LLNL and industry on the Extreme UltraViolet Lithography (EUV) program.

A.9.2 Microelectronics

The heart of SNL's microelectronics capability is the Microelectronics Development Laboratory (MDL), a modular 37,500 square foot facility with 12,500 square feet of Class 1 clean room space for processing wafers up to 150 mm in diameter (the MDL is gradually transitioning to 0.25 μm, 200 mm wafer technology). With a focus on digital devices, the MDL runs two full-flow CMOS technologies — 1.25 μm technology in support of smart technologies, sensors, micromachines and packages; and 0.5μm technology used primarily in advanced process development and IC equipment evaluation.

The primary function of the MDL is R&D and prototype production of radiation hardened (RH) ICs. SNL's RH/Custom Product infrastructure includes research and prototyping of advanced microelectronic packaging, high density interconnection, microsensors, micromachining, contamination-free manufacturing, microelectronic

fabrication equipment improvement, advanced materials, and advanced process development for the semiconductor industry. The MDL operates a complete equipment set to support its full-flow 0.5 μm and 1.25 μm processes. A partial list of MDL capabilities includes: submicrometer photolithography; plasma and reactive ion dry etch facilities; critical dimension metrology; 200 keV ion implanters, wet chemistry benches; oxidation and diffusion furnaces; low-pressure and plasma-enhanced chemical vapor deposition reactors (LPCVD and PECVD); sputtering and evaporation metallization systems; and inspection stations including scanning electron microscopes, surface particle detectors, and optical microscopes. The MDL Semiconductor Roadmap is described in Table A-3.

Table A-3. Sandia MDL Semiconductor Roadmap

Technology Feature	Year				
	1995	1998	2001	2004	2007
Bits/chip (SRAM)	256K	1M	4M	8M	16M
Chip Size (mm^2)	200	400	600	800	1000
Feature Size (μm)	0.5	0.35	0.25	0.18	0.10
Wafer diameter (mm)	150	200	200	200-300	200-300
Levels of metal	3	4-5	5	5-6	6
Defect density (#/cm^2)	0.8	0.4	0.25	0.15	0.05
Power supply voltage (V)	5.0	3.3	3.3	2.5	2.5

The MDL has developed and is advancing a broad range of sensor and actuators based on polysilicon surface micromachining. Chemical Mechanical Polishing (CMP) is being used to improve manufacturability and reliability of MEMS and has become a critical MEMS enabling technology. Both 1.25 μm and 0.5 μm CMOS technologies are used to create MEMS devices. A number of micromachined sensors are being developed including pressure sensors, accelerometers, volatile organic sensors combustible gas sensors, and atomic force microscope (AFM) sensors. Micromachined actuators have resulted in the development of a four-level polysilicon process which enables the fabrication of complex mechanical systems with micrometer feature sizes. Complex engines have been fabricated which are capable of operating at 300,000 rpm with lifetimes in excess of 3.2 billion revolutions. SNL is pursuing several technology development

efforts which enable the integration of electronic and micromachine structures (e.g., sensors and actuator mechanisms) on the same chip.

The Center for Microelectronics Technologies (CMT) was created by combining the MDL with a $20 million donation of IC processing equipment from the IBM Corporation. In combination with the MDL's extensive Class 1 clean room facilities, the CMT provides the equipment and technical staff to take concepts all the way from research and prototyping through testing and application.

The MDL/CMT is augmented by the Compound Semiconductor Research Laboratory and a range of microelectronics related "virtual centers" that draw resources from organizations throughout the laboratory. For example, in addition to MDL research on microsensors, the Microsensors Research and Development Department conducts research and development on a variety of sensor technologies including surface-acoustic-wave (SAW), fiber-optic, and field-effect-transistor (FET) sensors. Also, SNL's Analog Products Department provides customer-specific solutions in the areas of analog and mixed-signal ASICs, as well as circuit and system modeling. Specialized design, testing and packaging can be provided when standard procedures are unable to meet the customer's needs (e.g., classified radiation-hardened components). Production is performed by a commercial vendor after prototype testing has verified the design.

A.9.3 Electronics Integration Technology

SNL invests approximately $8-9 million annually in electronic packaging, with a current concentration on MCMs, test chips, and reliability. SNL's packaging capabilities span MCM development from concept to final production. SNL is working to advance MCM technology in modules produced in Low-Temperature Co-fired Ceramics (MCM-C), deposited MCMs (MCM-D), and laminate MCMs (MCM-L). All of these approaches have demonstrated significant advantages in size, weight, and performance over standard packaging solutions. In particular, research is under way at SNL to develop optoelectronic interconnects for signal transmission between levels in a 3-D package, and for the drilling and plating of conductive vias in substrates to provide power and ground connections between levels.

The Electronics Quality/Reliability Center (EQRC) has a complete industrial capability for reliability, failure analysis and test, with an installed base of equipment valued at $10 million and an annual budget of over $5 million. The EQRC includes a 5,000 square foot laboratory and 40 major pieces of equipment, most of which are

computer controlled. Areas of expertise and capability include: new failure analysis techniques, reliability test-lab-on-a-chip, assembly test chips, failure analysis using an expert system, and Iddq testing and burn-in elimination.

APPENDIX B. DOD NEEDS

The DOD science and technology needs have been articulated in the 1997 Defense Technology Area Plan (DTAP)[1]. This appendix presents excerpts from DOD needs focused on Defense Technology Objectives (DTOs). The DTOs are developed as technological opportunities for meeting the Joint Warfighting Capability Objectives (JWCOs). The DTOs relevant to microelectronics are summarized from the DTAP [DTAP 97] and presented in Section B.1. The current DOD investment strategy (as articulated in the DTAP [DTAP 97]) is a plan for achieving the objectives described in the DTOs and excerpts ([DTAP 97]) are presented in Section B.2.

B.1 DEFENSE TECHNOLOGY OBJECTIVES SUMMARY

B.1.1 Low-Cost Electronically Scanned Antennas (SE.01)

Overcoming the challenge of developing low-cost electronically scanned antennas (ESAs) for multiple platforms and applications will allow the warfighter to benefit from the acquisition of a significantly larger number of more capable systems in a time of declining resources. In FY97, the Army will be evaluating and developing scanning strategies for an antenna based on Rotman lens technology. In FY98, the Rotman lens design will be finalized, assembled, and tested. The program goal is to realize acceptable performance of an ESA at less than 50% of the current cost. The current antenna integration includes three parts: the Rotman lens, an Endfire "Vivaldi" notches aperture array, and a switch control matrix. The performance goals for this approach are a horizontally polarized antenna with an operating frequency range from 6 to 18 GHz, an azimuth field of view from 45deg, an antenna gain of 30 dB, and beamwidths of 2-deg azimuth and 6-deg elevation.

The Navy is investigating two candidate lens technologies (ferroelectric and diode) for reducing the cost and weight of X-band phased arrays, while still maintaining the required performance. In FY98, a 5" x 5" ferroelectric lens will be built and tested. Specific

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[1] Defense Technology Objectives of the JWSTP and DTAP, Department of Defense, Director, Defense Research and Engineering, January 1997

lens. Goals for this technology program are to achieve mission acceptable performance (platform dependent) at a procurement cost of less than 70% of current high-performance active element array costs. Cost savings goals are based on ESA capability with few or no transmit/receive modules. In the diode lens approach, the necessary phase gradient is introduced by turning diode strips located between parallel plates on and off to change the apparent dielectric constant. In FY98, a 4" x 8" diode lens will be tested as a radar with slotted array. Specific technology goals are 1-GHz bandwidth, insertion loss of less then 1.0 dB for the lens, and sidelobe degradation of less than 2 dB.

The Radar Systems Aperture Technology is an Air Force program for demonstrating technologies to reduce radar systems cost by 40% and improve radar systems reliability by 40%, while maintaining or improving overall system performance. Technologies being developed include continuous transverse stub (CTS) antennas made of voltage-variable dielectric material. CTS antennas provide ESA performance at half the cost of active ESAs. A laboratory demonstration of the CTS antenna will be conducted in FY98.

B.1.2 Advanced Pilotage (SE.07)

To take the fight to the enemy without detection, the warfighter must enter and exit hostile areas at night and in adverse weather, using evasive maneuvers. The battle cannot be won until safe and survivable pilotage and navigation is first accomplished by all air and surface craft. This DTO develops and demonstrates advanced sensor technology for night/adverse weather pilotage/navigation requirements. Included will be all aspect viewing via fixed-mounted sensors providing full sphere coverage, large staring arrays, and multispectral image fusion. By FY97, the program will develop and flight test an image intensified sensor and fast IR focal plane array for a wide-field-of-view thermal sensor, demonstrating a 50% increase in obstacle recognition range in the poorest weather and in the darkest nights, a 25% increase in the instantaneous field of vision, and a decrease in the required number of training flight hours for "low time" aviators by 20%. By FY98, the goal is to demonstrate an integrated, wide-field-of-view pilotage/navigation sensor and display suite with image fusion. Image fusion combines the most salient features from the complementary FLIR and image intensified sensor imagery to show a single, complete picture of the operating area on a helmet-mounted display. This project will demonstrate a 25% decrease in target detection time using fused imagery.

B.1.3 Integrated Platform Avionics Demonstration (SE.23)

This DTO develops low-cost solutions for future tri-service retrofit and forward-fit applications in integrated avionics by utilizing tri-service development products in a series of testbed demonstrations. Areas of concern encompass system architecture, multifunction apertures, integrated RF and EO subsystems, core signal and data processing, vehicle management system, weapon stores management, power generation, and environment control systems. Tri-service transition vehicle opportunities would be JSF variants, NF–22, and current operational aircraft upgrades, both fixed wing and rotocraft. The objective is to lower entire life-cycle cost by attacking all aspects of the system acquisition process and many cost-inducing factors.

Two thrusts are currently underway supporting the DTO effort: the Maritime Avionics Subsystem Technology Program and the Aging Aircraft Avionics workshop held in September 1996 at WPAFB. The workshop, comprising corporate level representatives from the major aircraft prime contractors, depots, and Air Force commands, planned technology efforts to solve the upgrade and support issues for aging aircraft that will represent over 80% of the operational fleet for the next 35 years.

FY98 will develop individual enabling technology applications such as analog RF photonics, digital fiber optic networks, high-density electrical connectors, integrated sensor systems in the RF and EO domains, and digital IF processors. FY99–00 will produce "stairstep" demonstrations of system capability threads using incremental modeling and simulation integration demonstrations. The focus will include information fusion, portable operating systems, support software environments and COTS-based technology. These will be followed by incremental prototyping and integration demonstrations involving packaged hardware, reconfigurable or throw-away modules, and system software re-use. The final far-term demonstration will be real-time weapon system integration applications applied to a retrofit program for operational aircraft. Technology goals to be reached by FY00 include a 30% reduction in avionics suite cost (development, flyaway, and support) and reduced weight/volume/prime power by 30%. The tri-service testbed will allow timely integration of current enabling technologies and provide opportunities for tri-service access, common interface, and joint utilization of products.

B.1.4 Advanced Common Electronic Modules (SE.24)

The purpose of this effort, a new start in FY97 and funded under the Affordability Program, is to develop advanced common electronic modules consisting of two processing

families: common sensor interfaces acquiring data directly from the sensors of the electronic suite in a platform; and digital processing computing nodes sustaining increased performance in processing, communication input-output bandwidth, and latency. The modules developed will be smaller and have lower power consumption and higher performance, while accomplishing all the acquisition, transmission, and digital processing of RF signal electronics over a very wide frequency range (50 MHz to 45 GHz). This technology incorporates all RF signal electronics (transmitting and receiving) into a small set of modules for signal conditioning and subsequent signal processing. Advanced Common Electronic Modules (ACEM) builds on over a $100 million DARPA investment including the High-Performance Computing, Rapid Application-Specific Signal Processing, and Electronics Packaging and Interconnect Technology programs.

This program will eliminate most analog electronics and perform the functions digitally. To accomplish this, the following must be achieved: improved high-speed A/Ds and D/As, RF up-and-down converters, high-speed digital signal processors, and low-power electronics. All of the RF functions will be processed by a single device. The success of this program will result in a 5:1 reduction in wiring, a 10:1 reduction in weight and power, and an 8:1 reduction in life-cycle cost (LCC) for electronic modules.

Trade-off studies will be performed to define critical design parameters affecting requirements for system applications across the naval airborne, shipborne, undersea, and overhead platforms involving RF sensors, interfacing, and data processing assets. Once this is completed, a system design document describing recommended architecture(s) and function performance parameters will be developed, followed by advanced development models for an integrated processor. Demonstration tests initially will be performed in the laboratory and then in an SH–60R helicopter for flight testing.

Milestones include, in FY97, components validation, module design, and LCC modeling; in FY98, module design and prototyping and LCC module validation; in FY99, module assembly, fabrication and integration, and laboratory tests; and, in FY00, SH–60R installation and SH–60 flight demonstration.

B.1.5 SE.26.01 Millimeter-Wave Power Modules (SE.26)

The objective of the MMPM effort is to develop a compact, lightweight, highly efficient transmit/receive module operating in the 18–40-GHz frequency range. The module technology is intended to support ongoing and planned communications and electronic warfare systems, as well as being compatible with application in multifunctions electroni-

cally steered, active arrays. The primary technical challenges encountered in this development are driven by the need to obtain efficient power production in a small package and to obtain a proper balance between performance and affordability. As with the microwave power module, the approach is to distribute the RF gain between the solid-state driver and the vacuum power booster to reduce the size, increase the efficiency, and reduce the noise performance of the module. The MMIC driver, vacuum amplification stage, and electronic power conditioning are optimized for functionality and efficiency. The need to respond to specific applications at an affordable cost determines the module configuration. Deliverables within this effort include delivery of two (Raytheon) and ten (Litton) MMPMs (transmit only) in FY97. Initial evaluation of the MMPM technology for electronic warfare is planned for FY98 with the implementation of a 1 x 8 active, electronically steerable array (NATO TRIAL MACE test) and an ALE–50-based MMPM towed decoy. Specific metrics for the MMPM effort are a wideband efficiency of greater than 30% and output powers greater than 45 W. This DTO supports JWCO Information Superiority (A.10, High-Altitude Endurance Unmanned Aerial Vehicle ACTD, and A.13, Satellite C3I/Navigation Signals, Propagation Technology), Combat Identification, Electronic Combat, and Joint Theater Missile Defense.

B.1.6 Microwave SiC High-Power Amplifiers (SE.27)

This DTO will develop compact, lightweight, highly efficient L- through X-band microwave solid-state transmitter building blocks for potential use in high-performance radar, communications, and electronic warfare systems. It will develop advanced silicon carbide (SiC)-based field effect transistors (FETs) and static induction transistors (SITs) that meet output power, power density, efficiency, linearity, operating voltage, and temperature to provide size, reliability, and life-cycle cost advantages over competing Si and GaAs-based solid-state amplifiers and tube-based RF transmitter systems. The program will further optimize SiC substrate and epitaxial material growth, device processing techniques such as ion-implantation, reactive ion etching, ultraviolet lithography, and contact metallization; and establish advanced device and amplifier design and simulation tools to reduce costs. A goal is to develop high-temperature and high-thermal conductivity interconnect and packaging technology to accommodate high-temperature applications and greater power dissipation levels. In FY97, the program will complete development of (1) 75-W S-band power SIT and 10-W X-band SiC MESFET, and (2) high-temperature interconnects as needed for SiC MMICs. The FY98 goal is development of 150-W S-band SIT and 25-W X-band MESFET. The program will demonstrate, by FY99, the applicability of

a wide bandgap material, SiC, to prove high-power microwave amplifiers by demonstrating a 300-W S-band SIT and 100-W 10-GHz hybrid amplifier. This DTO directly supports the Air Force's AN/TPS–75 ground-based radar transmitter upgrade, impacts Army Patriot, GBR, and THAAD systems, as well as ground-based, shipborne, and airborne surveillance and fire control radars and EW jammer equipment. Other systems directly affected are the Navy SHF rapid deployment system, FAST SATCOM system, and Sea Sparrow transmitter. This DTO supports JWCO Information Superiority, Electronic Combat, and Joint Theater Missile Defense (D.04, Advanced X-Band Radar Demonstration).

B.1.7 Low-Power Radio Frequency Electronics (SE.28)

Man-portable communications and advanced airborne and space-based platforms are severely limited in volume and weight. In addition, the demands for wider bandwidth, higher stability, and increased functionality are challenging available technology. New lower power RF devices and components are needed to improve sensitivity and selectivity with reduced noise, while minimizing power consumption in planned and ongoing communications and sensor-based systems. This DTO encompasses design, fabrication, and simulation of device structures, circuits, and materials for power-efficient RF electronics, high-power added-efficiency amplifiers and sources, ultra stable frequency control oscillators and clocks, miniaturized low-loss filters and microresonators, circulators, and enhanced component thermal management technologies. In FY97, the program will develop low-power consumption GaAs RF ICs for advanced receivers with emphasis on use of heterojunction ICs for low-noise amplification over wider bandwidths. In FY98, the goals are to develop and demonstrate a low-noise, low-acceleration sensitivity frequency source with a fivefold improvement in acceleration sensitivity for improved slow-moving target detection capability (e.g., in JSTARS, by optimizing acoustic mode shape and device geometry); and to develop multifunction communications and radar ICs and subsystems for advanced receivers to achieve a fivefold reduction in power consumption, demonstrate miniature filters integrated into multifunction transmit/receive module assemblies, and conduct demonstrations of miniature digital receivers aimed at increasing performance at a reduced cost, size, and weight for radar/EW multifunction systems. By FY99, the program will demonstrate a low-power, high-accuracy clock that is five times smaller, two times lower power, and two times higher accuracy for jamming-/spoofing-resistant GPS receivers; and demonstrate small, man-transportable, extended autonomy-period MILSTAR terminals by exploiting new piezoelectric materials such as langasite and lithium tetraborate in addition to novel resonator structures. This DTO supports F–22 radar and EW, GBR, GEN-X, GPS, CEC,

MILSTAR, Scamp, Longbow, BCIS, SADARM, STAFF, and BAT. The following JWCOs are supported: Information Superiority (A.13, Satellite C3I/Navigation Signals Propagation Technology), Precision Force (B.03, Precision Signals Intelligence Targeting Systems ACTD, and B.05, Target Acquisition ATD), Combat Identification (C.01, Battlefield Combat Identification ATD), Electronic Combat, Joint Theater Missile Defense (D.04, Advanced X-Band Radar Demonstration), Military Operations in Urban Terrain (E.01, Small Unit Operations TD), and Joint Countermine.

B.1.8 Design Technology for Radio Frequency Front Ends (SE.29)

This DTO will develop tools and processes for the rapid and efficient design of monolithic microwave integrated circuits, multichip assemblies, and mixed signal electronic subsystems for use in high-performance electronic warfare, radar, and communication systems. The overall goals are to drive down system front-end costs, to increase system front-end capabilities, to enhance system portability, to upgrade reliability, and to reduce life-cycle costs. The MAFET Design Environment will help accomplish the above cost objectives by reducing RF multichip assembly module development from the present 20 man-years of effort to 6, and the cycle times from over 3 years to 1 by FY99. The number of design cycles will be reduced by providing more accurate models and developing a behavioral modeling capability to support earlier, system-level design space exploration (virtual prototyping). The time per design cycle will be reduced by developing faster simulation tools and better integration of design tools to allow more portability of designs and models among the tools. Front-end performance capability will be improved by providing the virtual prototyping to allow more realistic trade-offs of system performance requirements with hardware capability. The approach is to provide enhancements and new developments by the leading computer-aided engineering (CAE) tool suppliers to address the above objectives, with tight coupling to the microwave/millimeter wave industry, and to establish processes to ensure end-user requirements are addressed. The mixed signal design system will enable the synthesis and simulation of digital signal processing hardware, software, and components in one application. The resulting capabilities will become part of the commercial product lines of these leading CAE system suppliers and will therefore be sustained after the government-sponsored program ends. In FY97, the program will release design environment interoperability specifications. In FY98, the program will release the beta version of design environment to all benchmark sites and demonstrate mixed signal coupling and contamination analysis software. In FY99, the final version of design environment for mixed-signal RF front-end designs will be evaluated. This DTO supports F–22

radar and EW, GBR, MILSTAR, Scamp, Longbow, BCIS, SADARM, STAFF, BAT, Aegis SPY–1D upgrade, ALQ–131, and ALQ–136. The following JWCOs needs are supported: Information Superiority, Precision Force, Combat Identification, Electronic Combat, Joint Theater Missile Defense, Military Operations in Urban Terrain, Joint Countermine, and Joint Readiness and Logistics.

B.1.9 High-Density Radiation-Resistant Microelectronics (SE.37)

High-performance, extremely dense, radiation-resistant microelectronics are key to continued U.S. domination of battlefield surveillance, intelligence, and communications, as well as joint theater missile defense. This DTO focuses on providing space and strategic systems with timely access to affordable state-of-the-art, radiation-resistant microelectronics. Space applications, which presently dominate requirements for radiation-resistant microelectronics, need to operate reliably after exposure to natural and nuclear radiation (e.g., total dose greater than 300 krad, dose rate upset thresholds greater than 10^8 rad/sec, SEU thresholds greater than 40 MeV/cm^2/mg). These systems also demand significant reductions in weight, size, and power while simultaneously increasing performance. Customers for radiation-resistant microelectronics include strategic missiles (Minuteman and Trident), BMDO interceptor systems, and satellites such as MM-III GRP, EKV, MILSTAR, UHF follow-on, GPS-IIF, DSP, SBIRS-High, SBIRS-Low (SMTS), and Advanced EHF.

Specific technology objectives include demonstration of power converters with 95% efficiency by FY97; demonstration of a radiation-hard, single-chip, 16-bit silicon-on-insulator (SOI) processor for strategic missile applications by FY97; development of a submicron radiation-resistant microelectronics fabrication process to produce a 16 times increase in density, and enable development of a 32-bit data processor by FY98 and a radiation-resistant 4-Mb static memory by FY99; demonstration of a 256 k-bit nonvolatile memory by FY99; and development of an extremely high-density, mixed-signal sensor processor that incorporates next-generation packaging concepts by FY99.

B.1.10 Microelectromechanical Systems (SE.38)

MEMS components are expected to improve the size, weight, cost, and assembly complexity of existing applications areas such as positioning systems and inertial guidance systems by an order of magnitude. MEMS promises to allow new programs started in the near term to deploy accelerometer, GPS, and inertial guidance functions an order of magnitude lower in size, weight, cost and assembly complexity than alternative technologies. Key near-term challenges are to develop the basic materials, devices, and processes to inte-

grate mechanical components at a density of 1,000 mechanical components/cm^2 with on-chip microelectronics of at least 10,000 transistors. A basic support for this technology area will be the development of an infrastructure that not only can build single prototype components at increasing densities and complexities, but also lays the foundation for establishing a reliable, assured industrial base to supply emerging defense applications.

Specific technology objectives include development of an integrated inertial guidance system on a chip in FY97; demonstration of a high-performance accelerometer that is monolithically integrated with electronics exhibiting ten times improvement in stability and sensitivity over current accelerometers in FY98; and demonstration of integration densities of 500 integrated mechanical components/cm^2 in FY98, and densities of 1,000 integrated mechanical components/cm^2 in FY99.

B.1.11 Wide-Bandgap Electronic Materials Technology (SE.39)

This DTO develops high-performance, wide-bandgap semiconductor materials for advanced compact transmitters used in military-essential RF radar, communications and electronic warfare sensors, and compact laser sources and detectors. The availability of silicon carbide wafers compatible with commercial semiconductor processing technology is essential to ensure an adequate yield of devices to meet systems performance/cost requirements. Attainment of the silicon carbide goals will enable production of high-power switches operating at greater than 1,000 V and at current densities exceeding 1,000 amps/cm^2. The resultant power density exceeds that of silicon by a factor of five, achieving considerable size and weight reduction of power supplies in support of all electric ships and more electric aircraft. Development of SiC, GaN, and AlN will enable implementation of 50-W, 18–40-GHz power modules for compact EW transmitters; blue light-emitting diodes with greater than 10,000 hours lifetime; blue and ultraviolet lasers with greater than 1,000 hours lifetime; and solar-blind ultraviolet detectors. In FY97, the program will complete development of 150-W SiC SIT, 25-W X-band MESFET, and high-temperature interconnects for SiC MMICs, as well as develop controlled p-doping of GaN epitaxial films. The FY98 goal is to demonstrate 3-in diameter substrate wafers of 4H and 6H silicon carbide with uniform doping and defect density less than $10^3/cm^2$ across the entire wafer, high-resistivity silicon carbide substrates, 150-W S-band SIT, and a 25-W X-band hybrid amplifier. Other FY98 goals include developing reproducible epitaxial growth of doped and semi-insulating, low-defect density (less than 105/cm2) GaN; and demonstrating reliable shallow p-type doping technology for epitaxial growth of GaN. In FY99, the program will develop a commercially viable epitaxy process that yields materials properties (defect den-

sity, control of dopants) that exceed substrate quality, demonstrate a 300-W S-band SIT and 100-W 10-GHz hybrid amplifier, develop a means to synthesize GaN substrates of 1 in or greater diameter, and develop effective doping of high aluminum alloy ratio AlGaN material.

B.1.12 Energy Conversion/Power Generation (SE.43)

This DTO will demonstrate small, lightweight, low-cost, environmentally compatible power sources with high power and energy densities by providing, in FY98, at least a 50–100% increase in energy density for electrochemical, electromechanical, and other direct energy conversion devices. This advance in energy density will enable corresponding reductions in portable power source size and weight (30–50%), and support increase power demands for man-portable electronics, sensors, lightweight TOCs, etc. This will contribute to the military's ability to project mobile forces, execute longer missions, and provide power on the move. All efforts will improve the deployability, tactical mobility, and effectiveness of a CONUS-based fighting force.

The program will deliver next-generation primary batteries (30% increase in power density) for tactically mobile use in the 21st Century Land Warrior Field demonstration in FY98; deliver initial prototype fuel cells for field demonstrators to Dismounted Battlespace BattleLab (ACTII demonstration) and Special Forces Command (60% reduction in power source weight) in FY98; deliver next-generation 60-lb, diesel-fuel-burning, 3,000-W engine driven generator set for use in the Gen II and Hunter Sensor Suite ATDs in FY98; and demonstrate liquid-fueled fuel cell in FY99.

B.1.13 Power Control and Distribution (SE.44)

Advanced military platforms are becoming near all-electric to meet mission performance and requirements. To meet these challenging objectives in generating, converting, and distributing electric power requires the minimization of the cost, weight, and volume/size of power electronics while maximizing performance—the product of current density, standoff/blocking voltage, and turnoff time or switching frequency. These advanced systems anticipate tenfold improvements in power density and a factor of 3–5 in the reliability and switching speed for power electronic building blocks (PEBBs) over the present-generation conversion and distribution systems technology. The power, control, and distribution (PCD) envelope must encompass commonality, performance (e.g., power density, affordability, maintainability), and dual-use applicability. Meeting the PCD goals for FY00 and FY05 will require advancements in power switching devices and diodes, gate drivers and

power control electronics, power circuit and topology, packaging, and thermal management technologies. Significant military capabilities in consort with industry commercial market, will provide for flexibility and commonality through the development of the smallest number of PEBB components for the largest number of applications. This DTO develops technologies to revolutionize, through the use of PEBBs, the way electric power is produced, stored, distributed, and used using the U.S. industrial infrastructure for volume manufacturing, and it achieves reduced cost for military and private sector applications.

The program demonstrates a 100-W, 50–3.3-Vdc, high-efficiency, high-density, low-voltage power that operates at 1 MHz with a conversion efficiency of 90% in FY97. Further advances in the use of wide bandgap materials for power applications will realize additional improvements in conversion efficiency while increasing switching speeds to as high as 100 MHz by FY00. The program also will demonstrate PEBBs for application in advanced shipboard for a "More Electric Navy" (e.g., SC–21, airborne, combat systems, vehicular platforms), providing ten times improvements in power conversion, distribution efficiency, power density, and switching speeds that reduces the size, weight, and cost; and a three to five times improvement in reliability by FY00. A goal is to provide 90% reduction in cost for power, using digital-controlled elements.

B.1.14 Space Radiation Mitigation for Satellite Operations (SE.55)

The increased dependency of the DoD on space-based assets makes it imperative that these space systems provide uninterrupted support to military operations. Satellite operations are adversely affected by space radiation, which can cause transients in, or failure of, sensitive electronic components and premature degradation of space power systems and other satellite systems. The objectives of this DTO are (1) to establish the causal relationship between the space radiation environment, satellite anomalies, and satellite systems degradation and failures, and (2) to develop techniques and instrumentation to mitigate these adverse effects of the space radiation or to provide alerts of the occurrence of hazardous space environments. The technology challenges addressed by this DTO are (1) to validate the effectiveness of the charge control system (CCS) technology to autonomously detect and eliminate the occurrence of high-voltage charging on operational satellites and thus eliminate the hazard such charging poses, (2) to demonstrate in space highly miniaturized operational sensors systems for real-time alerts of space environmental hazards, and (3) to develop and fly a compact system to determine routinely the space environmental hazards to new and emerging space technologies. The specific demonstrations supported by this DTO are the Compact Environmental Anomaly Sensor (CEASE) to provide real-time

alert, the Bulk Charging Hazards Interaction System (BCHIS) to determine charging hazards to new technologies, and the Photovoltaics Arrays for Space Power (PASP) testbed to determine the effects of the space environment on the performances and lifetimes of new and emerging space power technologies applicable to space-based radars (SBRs) and other high-power systems. The near-term vision is to have CEASE included as an in-situ diagnostic for all future military space systems.

Milestones include: in FY98, complete assessment of CCS mitigation techniques, with the elimination of all spacecraft charging hazards on operational satellites using CCS techniques; in FY99, demonstrate CEASE functionally in spaceflight, with a goal of 90% local specification of hazardous space conditions for operational satellites flying CEASE; and, in FY01, space flight BCHIS test system, showing a 25% increase in speed of application of BCHIS tested technologies to space system design.

B.1.15 Analog-to-Digital Converter (SE.57)

Significant advances have been and continue to be made in both silicon and III-V semiconductor IC technologies. DoD systems can reap the benefits of these emerging technologies in both retrofit and new programs. Emerging advances in IC technologies will allow the digital interface to migrate closer to the sensor/antenna in military receivers, reducing or completely eliminating the analog down-conversion stages that are bulky, costly, temperature sensitive, and require considerable calibration. This DTO focuses on the analog-to-digital converter (ADC), which is the key component for managing all sensor data in a wide range of areas (e.g., space-based electronics, ASW, smart weapons, C^4I). The capabilities of many defense systems are currently limited by the performance of their ADC, with particular known and projected threats in operational scenarios and jamming environments. Frequently, system requirements involve the fusion of several information processing and control functions that must be performed with real-time responses at very high rates (10–10,000 GFLOPs) while striving to increase the reliability/manufacturability of the system and simplify both the receiver and the transmitter. The primary objective of this DTO is to develop ADCs and related components to demonstrate digital receivers targeting military radar, EW, and CNI systems with the initial demonstrations in digital receivers and EW radar (E2C and AWACS). Some specific impacts of these developments and demonstrations are a 16 times improvement over current 1996 capabilities in over-the-horizon detection, detection of a submarine periscope in clutter, and precision tracking of horizon sea-skimming cruise missiles in clutter. Programs that are expected to employ these technologies include the F–22, Comanche, JSF, Aegis SPY 1–D, F–15 APG–63 upgrade,

F–18 APG–73 upgrade, E2C APS–145 surveillance radar, and B–2 APQ–181 radar. Specific development objectives include an 8-bit, 3-Gsps and a 12-bit, 100-Msps GaAs HBT ADC by FY97; a very accurate 16-bit, 125-Msps ADC in CMOS/SOS by FY97; a 10-bit, 1-Gsps GaAs HBT ADC by FY98; and a 4-bit, 20-Gsps ADC implemented in CMOS/SOS by FY99.

The goal is application of these advances for down conversion with an InP HBT bandpass Δ-Σ modulator for a double down-conversion receiver (180-MHz center frequency) by FY97, with improvements for a single down-conversion receiver (1-GHz center frequency) by FY98, and a direct conversion receiver (10-GHz center frequency) by FY99.

B.2 DEFENSE TECHNOLOGY AREA PLAN SUMMARY

B.2.1 RF Components

The successful pursuit of national objectives requires the continued superiority of our military-essential RF electronics. The widening variety of military missions challenges these systems to be increasingly flexible, timely, and precise on their application. The RF components' sub-thrust is meeting this modernization challenge by developing affordable electronics technology for information dominance and improved dexterity in national strategy and response actions.

Radar remains DoD's primary all-weather sensor to provide capabilities such as surveillance, situation awareness, self and area defense, targeting, terminal guidance, and battle damage assessment. In addition, a major complement to the hardkill capability of weapons is the softkill afforded by EW systems that can potentially handle a much larger attack force than hardkill weapons. Finally, the glue that holds all these capabilities together to form an effective warfighting force is the communications networks. These three areas rely heavily on and are enabled by RF technology, which represents the key to force multiplication (the ability of a minimal number of U.S. platforms and personnel to defeat a much larger enemy force) and the avoidance of technological surprise on the battlefield. The following Joint Warfighting Capability Objectives are supported: Information Superiority, Precision Force, Combat Identification, Electronic Combat, Joint Theater Missile Defense, Military Operations in Urban Terrain, Joint Countermine, and Joint Readiness and Logistics.

The availability of affordable, manufacturable RF electronic components that satisfy the performance, weight, size, interoperability, cooling, and maintainability require-

ments of military systems is vital for sustaining the competitive edge of U.S. forces over their adversaries. These warfighting capabilities require reductions in size, weight, volume, power consumption, and costs. Advanced high-performance and affordable RF solid-state, vacuum electronic, frequency control, and antenna technologies are currently being transitioned into a broad range of military systems, including the F–15/ALQ–135, LANTIRN, AMRAAM, MILSTAR, GEN–X, GBR, GPS Longbow, Patriot, SADARM, Scamp, Staff, and F–22 radar and EW arrays.

The RF components thrust involves the technology required to generate, control, radiate, receive, and process VHF, UHF, microwave, and millimeter-wave signals. The technologies under development are applicable to solid-state and vacuum electronic devices, low-noise signal and frequency control components, microwave power modules (MPMs), monolithic microwave integrated circuits (MMICs), transmit/receive (T/R) modules, advanced packaging and interconnect technology, and antennas. The five technology thrusts that compose the RF component subarea are solid-state electronics, vacuum electronics, signal and frequency control, antenna support, and multichip assemblies.

B.2.2 Electro-Optics

The detection, precise location, specific identification, and tracking of targets and an accurate battlefield damage assessment are key elements of the JWCOs of Information Superiority, Precision Force, Combat Identification, Joint Theater Missile Defense, Military Operations in Urban Terrain, Electronic Combat, and Counter Weapons of Mass Destruction. Electro-Optics (EO) offers advanced technology solutions to the problems of high-resolution target location and identification, nighttime surveillance, and high-capacity data storage and processing. In addition, electro-optics is the basic technology of displays, which are crucial to all man-in-the-loop systems. The continued development of high-performance, man-in-the-loop, and autonomous systems using advanced EO technology will substantially advance global surveillance and communications; all-weather, day/night, camouflage-resistant precision strike missions against fixed and mobile targets; advanced antisubmarine warfare capabilities; and space and sea control systems.

High-performance sensors, displays, and data storage and processing will be required to meet future warfighter needs. Photonics will provide high-capacity, rapid-access data storage; distortionless wideband analog fiber optic communications for sensor, emitter, and antenna remoting; ultra high speed data processing for real-time analysis of SIGINT and ELINT data; and new approaches to steering and control of microwave beams.

Display technology will address the problems of developing high-definition, helmet-mounted displays for the individual soldier and the aircraft pilot. A short-term goal is to demonstrate the capability of the active matrix electroluminescent display (AMEL) to operate with analog inputs for low power and compatibility with existing signal sources. Cost reductions in IRFPAs will be sought through uncooled sensor technology and by improvements in the functionality of cooled IRFPA technology. New applications will be addressed through development of multispectral sensors. Laser technology will attempt to lower the cost per watt of semiconductor lasers, develop long-lived blue laser diodes, and demonstrate eye-safe tunable monomode optical fiber lasers. Specific goals include integration of IRFPA and ATR functions, 3D stereoscopic displays, and monolithic optoelectronic integration leading to 2D optical "smart" pixel arrays for high-speed parallel processors.

B.2.3 Microelectronics

The warfighter has become critically dependent on the ability of systems to process, store, and transmit information to achieve force multiplication through remote and distributed awareness and control. Key military equipment (e.g., sensor packages, satellites, man-portable communications equipment) must meet stringent military requirements as described in *Joint Vision 2010* (e.g., radiation and high-temperature environments, extended operating lifetimes, lower weight, high performance) to achieve force multiplication throughout the range of potential warfighter environments. A crucial factor affecting DoD's ability to provide superior capabilities to the warfighter is the cost of electronic systems, which depends directly on the producibility, quality, and cost of microelectronics devices, circuits, and fabrication technologies. The challenge facing DoD is to formulate an investment strategy that leverages the more than $150 billion commercial microelectronics market while still maintaining technology leads in low-volume areas that are key to military applications.

Over the short term (1–2 years), electronic systems enabled by microelectronics should double the capability for processing information in the battlespace, while reducing cost, power consumption, and weight by a factor of two. In the mid term (3–5 years), it is expected that microelectronics will enable a doubling of sensing resolution, range, or speed; reduce power consumption by a factor of 10; and reduce weight by a factor of 10. In the long term (6–10 years), microelectronics innovations should provide an order-of-magnitude improvement in the range of sensing capabilities, while decreasing cost, power consumption, and weight by more than a factor of 100.

The technologies for signal conversion and processing, low-power, radiation-resistant microelectronics, and microelectromechanical systems (MEMS) all have the potential to significantly increase the capabilities of weapon platforms and information systems and simultaneously decrease their size, weight, cost, and assembly complexity. The dramatic rate of microelectronics technology innovation has also created the need to ensure that the warfighter has access to current state-of-the-art microelectronics to sustain superiority. Toward that end, the rapid transition of new technology to the industrial base and insertion of new (possibly commercial) technologies into military systems will continue to play an increasingly important role in meeting future warfighter needs.

The microelectronics technology is geared toward meeting very unique military requirements through the exploitation of pivotal technologies based on a range of electronic materials (e.g., silicon and its compounds SiGe and SiC; GaAs and other III–V compounds) and novel processes for new device structures (e.g., MEMS and radiation-resistant components) and circuit applications (e.g., A/D converters and inertial measurement systems). Military use of these technologies, associated with deep submission, 250-nm feature sizes, will enable order-of-magnitude advances in sensors, low-power systems, and complex, radiation-resistant integrated electronic functions (for signal conversion, processing, amplification, and microelectromechanical sensing). These are to be implemented with advanced design architecture. This will allow handling of 10–1,000 times more data at several hundred times higher throughput through parallelism, functional density, and device speed, and covering a broad spectral range from dc to several tens of gigahertz.

The United States must maintain its military superiority in an era of rapidly changing microelectronics technology. This superiority is based on (1) force multiplication through advanced microelectronics (technology and component applications) with a minimum number of platforms and personnel, and (2) actively avoiding technological surprises in future combat scenarios. In this context, the microelectronics subarea develops device, circuit, and fabrication technologies to realize digital, analog, and mixed-signal integrated circuits that are needed for introduction in a timely and planned fashion into weapon systems ensuring superiority over our adversaries.

B.2.4 Electronic Materials

Warfighters are increasingly exploiting electronic systems to achieve force multiplication. The performance and price of components in these systems depend directly on the reproducibility, quality, and cost of electronic materials synthesis and processing. Electron-

ic materials science also is the enabling technology for electronic and EO devices, whose payoffs include higher maintainability, lighter weight, smaller volume per function, higher data rate processing, and higher frequency/bandwidth operation–characteristics essential for establishing military dominance in areas such as avionics, radar, C4I, guidance, target identification, surveillance, and navigation. For example, development of III–V semiconductor substrate and films/nanostructures will make more compact radars and higher frequency and data rate communication systems possible in the midterm (3–5 years). In the mid and long terms, materials for IRFPAs will make possible modules capable of broader band detection, multiple color response, and room temperature operation; wide-bandgap semiconductors will make electronics available that operates at 300–500 deg C (e.g., near engine components), as well as compact ultraviolet laser systems for full-color display applications and high-density optical data storage. Because electronic materials technologies are inherently dual use, DoD programs will benefit civilian electrotechnology, whose enhanced capabilities will benefit military technologies in time.

The electronic materials subarea develops materials, fabrication processes, and device structures that are not supported commercially; are necessary for developing RF, microelectronics, and EO devices and components; and combine affordability with high performance for use in DoD systems.

B.2.5 Electronics Integration Technology

Many of the Joint Warfighting S&T areas require significant advancements in affordable high-performance electronics technology, a major challenge given the relatively small volume of specialized military parts needed compared to commercial production volumes. Specifically, miniaturized, power-efficient, reliable, high-performance circuitry is needed for Information Superiority, Precision Force, Joint Theater Ballistic Missile Defense, and Electronic Combat. Today, the cost, performance, size, weight, power consumption, testability, reliability, and maintainability parameters of military systems must all be dealt with on an integrated basis.

The electronics integration technology (EIT) thrust is critical to all electronic equipment as it affects the performance, reliability, affordability, power generation, conditioning, and distribution for virtually every type of system, both military and commercial. The thrust includes:

- Integrated design environment technology.

- Test, reliability, and quality assurance tools, methods, and standards aimed at enabling comprehensive synthesis, design, and diagnostics from the individual transistor to the assembled multiboard system.
- Packaging and interconnect technologies for mixed-signal assemblies containing analog, digital, microwave, millimeter wave, and optoelectronic devices in conjunction with microelectromechanical devices that will preserve device performance throughout an electronic system while increasing reliability and reducing size, weight, volume, and cost.
- Energy conversion and power generation including advanced batteries, fuel cells, engine-driven generators, capacitors, and other direct-energy conversion technologies for manportable C^4I, soldier systems, communications equipment, sensors, combat service support applications, lightweight tactical operations centers (TOCs), tactical power systems, and emergency power.
- Power control and distribution including power electronic building blocks (PEBBs), which will revolutionize the way electric power is produced, distributed, and used for land/air/underwater vehicle propulsion, tactical power systems, electric weapons and vehicles, emergency power, silent power generation, smart munitions, manportable C^4I, and soldier systems.

APPENDIX C. EXTENDED ULTRA-VIOLET LITHOGRAPHY

The DOE laboratories have been significant players in on-going research activities in extended ultra-violet (EUV) lithography. Extended ultra-violet lithography for mass producing integrated circuits is still in the research phase. According to one Lucent Technologies scientist, the laboratory work has demonstrated most of the basic science for EUV lithography.[1] The basic system is best described as a form of projection lithography with soft X-rays of wavelength of 13 nanometers (nm).

The Lucent experiments to date have been done at the Brookhaven National Laboratory synchrotron EUV photon ring.[2] This machine could not supply the production capability required for competitive lithographic printing rate during manufacturing of 10 square centimeters per second rate. However, these experiments have demonstrated writing 100-nm features on a silicon substrate. Lucent indicated it has actually demonstrated 50-nm minimum feature size silicon structures.[3]

Recently, Intel has proposed to the semiconductor industry a consortium to do the pre-competitive engineering to bring EUV research to a demonstrated engineering practice. The consortium would sponsor a three-year, $100 million project to produce a complete lithography demonstration based upon the following capabilities illustrated in Table C-1.

Table C-1. EUV Interested Organizations & Capabilities

Organization	Related Capability
Sandia National Labs	Laser Plasma Source for 13-nm photons[a]
Lawrence Berkeley Labs	13-nm reflective x-ray mask projection system
Lawrence Livermore Labs	Processing and metrology capability
Lucent Technology	Custom device and process capability

[1] Alastair MacDowell of Lucent, (516) 344-5334, is stationed at Brookhaven National laboratory synchrotron facility.

[2] Capable of photons from 1 nm to 20,000 nm.

[3] The 40-nm features could generate the smallest practical transistor. Smaller transistors would have insufficient electron-hole pairs to function in a statistically reasonable fashion according to MacDowell.

Table C-1. EUV Interested Organizations & Capabilities (Continued)

Organization	Related Capability
Intel Corporation	Processor device and process capability
Ultratech	Commercial lithography steppers

a. An alternative source would be to develop 600 MeV electron storage ring as a synchrotron photon source costing an estimated $25 million to produce, whereas the LPS has been estimated as a $1 million to $2 million photon source.

Two of the advantages in using EUV technology include (1) mask production requirements will likely be met with simply an incremental evolution of the mask industry, which would likely prefer a five-to-one reduction technology as compared to the 13-nm, hard X-ray one-to-one proximity mask technology currently funded by the Defense Advanced Research Projects Agency at IBM; and (2) the EUV reflective mask technology is based on layer mirror materials that provide up to 60% reflectance, thereby limiting practical reflective elements in a lithography system to no more than six sequential elements.

Table C-2 provides an evolutionary photon based lithography technologies status for mass production of integrated circuits.

Table C-2. Evolutionary Photon Lithography Status

Source Wavelength	Minimum Feature Size	Mask to Print Ratio	Status	Actual and Potential SM&E Manufacturers /Researchers	Notes
Optical	400 nm -500 nm	5:1	Bulk of current mass production		Lucent makes ASICs in this technology
Optical 365 nm	300 nm -350 nm	5:1	Current leading edge Microprocessor and DRAM products	ASM-L Nikon Cannon	Intel makes leading edge processors in this technology
248 nm	250 nm	4:1	Lab/demo	ASM-L Nikon Cannon SVGL	Phase shift masks, shipping laboratory analysis units

Table C-2. Evolutionary Photon Lithography Status

Source Wavelength	Minimum Feature Size	Mask to Print Ratio	Status	Actual and Potential SM&E Manufacturers /Researchers	Notes
193 nm	180 nm	4:1	Lab units on order, some early units shipped	ISI SVGL Nikon	Concern about lens and mask glass damage from laser
13 nm	50 nm	4:1	Research	Lucent DOE labs Ultratech (CRADA with DOE Lab LLNL) Zeiss (German) Intel Proposed Consortium	Concerns: very large investment required $300M - 500M, lens surface over full field
1 nm	unknown	1:1	Research	IBM Motorola (DARPA funding)	Possible candidate for high density DRAM technology

The industrial advisory board to the EUV project includes Intel, Lucent Technology, American Microdevices (AMD), Sematech, and a DOD representation.

Points of Contact

This research work is described in Optical Society of America (OSA) publications, within the last 18 months. The team is a collaboration of DOE laboratories and Lucent Technology. The point of contacts at these organizations are found in Table C-3.

Table C-3. EUV Points of Contact

Company/Organization	POC	Telephone
Lucent Technology[a] @BNL	Alastair MacDowell	(516) 344-5334 (516) 344-5513 lab
Sandia National Laboratory (Livermore)	Richard Stulen	(510) 294-2070

Table C-3. EUV Points of Contact (Continued)

Company/Organization	POC	Telephone
Lawrence Berkeley Laboratory	Dave Atwood	(510) 486-4463
Lawrence Livermore National Laboratory	Don Kania (acting)	(510) 422-8213
Intel Corporation/R&D	John Carruthers	(408) 765-2950

a. Previously AT&T Bell Laboratories, now part of Lucent Technology

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LIST OF ACRONYMS

AEM	Analytical Electron Microscope
AFM	Atomic Force Microscope
AGED	Advisory Group on Electronic Devices
ALERT	Air Land Enhanced Reconnaissance and Targeting
ALS	Advanced Light Source
AMD	American Microdevices
ANL	Argonne National Laboratory
APFIM	Atom Probe Field Ion Microscopy
BIST	Built-In-Self-Test
BMDO	Ballistic Missile Defense Office
BNL	Brookhaven National Laboratory
BRP	Basic Research Plan
CAD	Computer-Assisted Design
CCST	Center for Compound Semiconductor Technology
CNVS	Color Night Vision System
CMO	Center for Microelectronics and Optoelectronics
CMP	Chemical Mechanical Polishing
CMT	Center for Microelectronics Technologies
COTS	Commercial-Off-The-Shelf
CRADA	Cooperative Research and Development Agreement
CXRO	Center for X-Ray Optics
CVD	Chemical Vapor Deposition
DOD	Department of Defense
DOE	Department of Energy
DARPA	Defense Advanced Research Projects Agency
DDR&E	Deputy Director for Research and Engineering
DNA	Defense Nuclear Agency
DSWA	Defense Special Weapons Agency
DSTS	Defense Science and Technology Strategy

DTAP	Defense Technology Area Plan
DTO	Defense Technology Objectives
E&M	Electromagnetic
EO	Electro-optical
EQRC	Electronics Quality Reliability Center
ETC	Echo Tracking Classifier
EUV	Extended Ultra-Violet Lithography
EXAFS	Extended X-ray Absorption Fine Structure Spectroscopy
FET	Field Effect Transistor
FPA	Focal Plan Array
GILD	Gas Immersion Laser Doping
GPS	Global Positioning System
HMDS	Helmet Mounted Display
IC	Integrated Circuits
IMEM	Integrated MEMS
IRFPA	Infrared Focal Plane Array
IRST	Infrared Search and Track
JWCO	Joint Warfighting Capabilities Objectives
JWSTP	Joint Warfighting Science and Technology Plan
KCP	Kansas City Plant
LANL	Los Alamos National Laboratory
LBNL	Lawrence Berkeley National Laboratory
LLNL	Lawrence Livermore National Laboratory
LPCVD	Low-Pressure Plasma-Enhanced Chemical Vapor Deposition
MCM	Microcircuit and Multichip Module
MDL	Microelectronics Development Laboratory
MEMS	Microelectronics
MMIC	Monolithic Microwave Integrated Circuit
MPM	Mechanical Property Microprobe
NCEM	National Center for Electron Micropscopy
NEXAFS	Near-Edge EXAFS
NRE	Non-Recurring Engineering
NSLS	National Synchrotron Light Source
OMCVD	Organo-Metallic Chemical Vapor Deposition
OMIC	Opto-Microwave Integrated Circuit

ORNL	Oak Ridge National Laboratory
OSA	Optical Society of America
PEBB	Power Electronic Building Block
POM	Program Objective Memorandum
RASSP	Rapid Prototyping of Application Specific Signal Processor
RSTA	Reconnaissance, Surveillance, Tracking and Acquisition
RTT	Resolution Tunneling Transistor
S&T	Science and Technology
SAW	Surface Acoustic Wave
SEM	Scanning Electron Microscopy
SNL	Sandia National Laboratory
SRC	Semiconductor Research Corporation
STARs	Special Technology Area Reviews
SEXAFS	Surface EXAFS
TAP	Technology Area Planning
TAR	Technology Area Review

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This study examined how key selected Department of Energy (DOE) laboratory capabilities align with Department of Defense (DOD) microelectronics requirements. DoD microelectronics, electronic materials, and electronic integration technology requirements were identified in the annual Defense Technology Area Plan (DTAP). An analysis of open information was used to select the key DOE laboratories with focused activities in the microelectronics area. The selected organizations were visited by the study team. The resulting analysis shows that the selected DOE laboratories and facilities have strong microelectronics capabilities in a wide range of areas relevant to the DTAP areas examined. A number of opportunities are identified for cooperative DOD-DOE microelectronics activities. Recommendations are made on areas of further analysis particularly in better coordinating and managing the defense interests across agencies.

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